



Prifysgol Cymru
Y Drindod Dewi Sant
University of Wales
Trinity Saint David

Examiner Only

Examination Answer Books

12 Pages

Instructions to Candidates

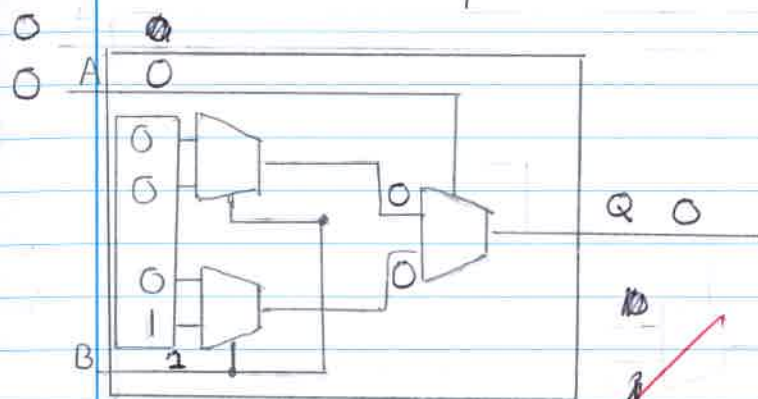
1. Please give the information requested in the boxes below.
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1	Student Number	2106959
2	Title of Examination Paper	Electronics II
3	Module Code	ACDAG001
4	Date and Time of Examination	10/05/23 9:00
5	Examination Venue	Swansea
6	Seat Number	044
7	Number of Answer Books handed in	1

[illegible]

(Gweler yr ochr arall am y fersiwn Cymraeg)

Q6) An LUT is a look up table used as a programmable logic block within FPGA. It contains a series of mux's as shown in the diagram below. When the select input to a mux is 1 the first input is outputted, when the select input is 0, the second input value is outputted.



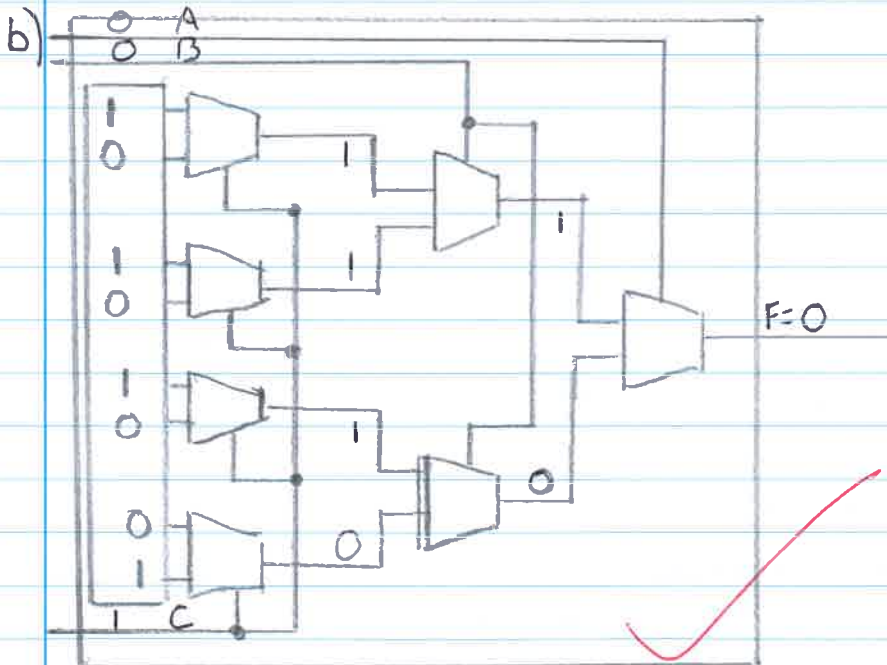
A binary value is stored in the register, such as '00011011' and is supplied by 3 inputs on this 3 variable LUT. If the supplied input is 001, A being 0, B being 0 and C being 1. The resultant output is as shown in the diagram above, Q will equal 1. '0001' and is supplied by 2 select inputs on this 2 variable LUT. If the supplied input is '01', A being 0 and B being 1. The resultant output is as shown in the diagram above, 'Q' the output, will equal '0'.

Q6)

$$ii) f = \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$$

a) Truth table

A	B	C	F
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1



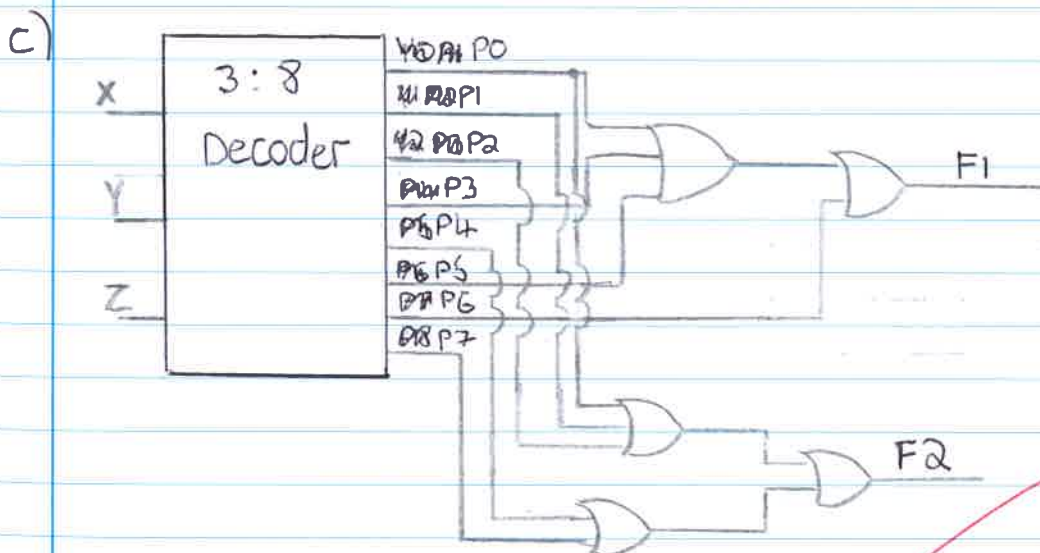
Q5)

a) $F1 = \sum m(0, 3, 5, 6)$ and $F2 = \sum m(0, 1, 2, 4, 7)$

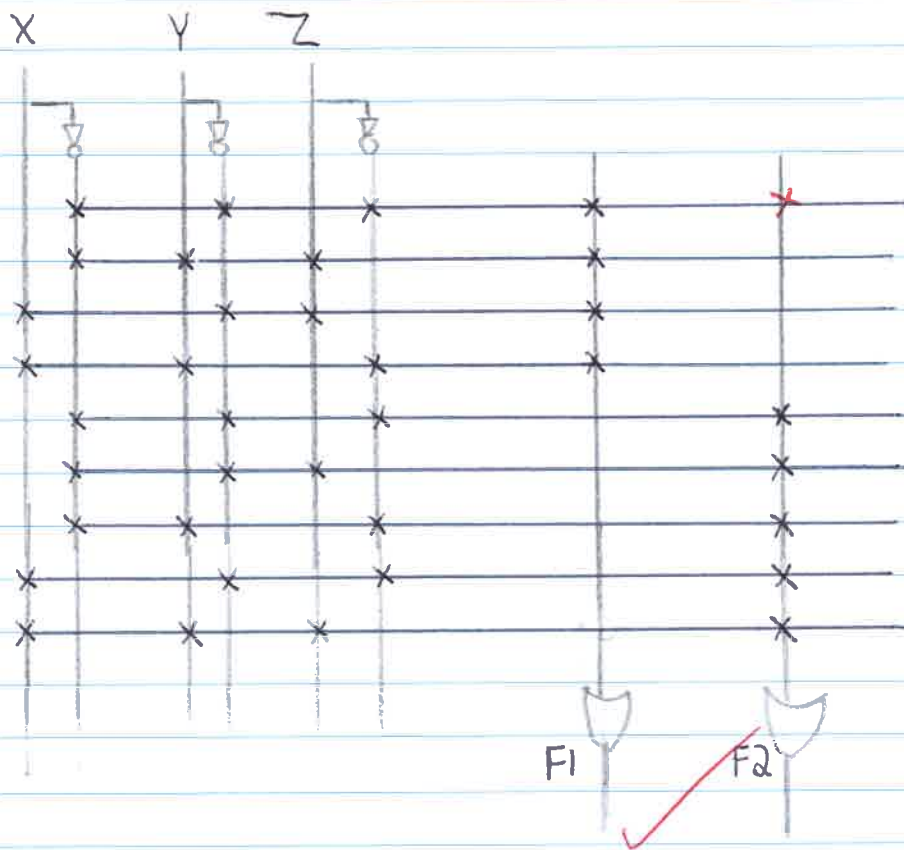
	X	Y	Z	F1	F2
0	0	0	0	1	1
1	0	0	1	0	1
2	0	1	0	0	1
3	0	1	1	1	0
4	1	0	0	0	1
5	1	0	1	1	0
6	1	1	0	1	0
7	1	1	1	0	1

b) $F1 = \bar{X}\bar{Y}\bar{Z} + \bar{X}YZ + X\bar{Y}Z + XY\bar{Z}$

$F2 = \bar{X}\bar{Y}\bar{Z} + \bar{X}\bar{Y}Z + \bar{X}Y\bar{Z} + X\bar{Y}\bar{Z} + XYZ$



Q5)
d)



5

19
20

Q3 & 4)

in

a) -5×4

$4 = 0100$

$5 = 0101$

$-5 = 1010$ is complement

2's complement

$$\begin{array}{r} 1010 \\ + 1100 \\ \hline \end{array}$$

$$\begin{array}{r} 1010 \\ + 1101 \\ \hline \end{array}$$

$$\begin{array}{r} 0100 \quad 1101 \\ \quad \quad 0100 \times \\ \hline 00000000 \\ 00000000 \\ 11111001 \\ 00000000 \\ \hline -20 \quad 11110100 \end{array}$$

$$\begin{array}{r} 00000000 \\ 11111000 \\ \hline \end{array}$$

$20 = 00010100$

$-20 = 11110100$

$$\begin{array}{r} 11110101 \\ + 11110100 \\ \hline \end{array}$$

$$\begin{array}{r} 1100 \\ 0100 \times \\ \hline 00000000 \\ 00000000 \\ 11110000 \\ 00000000 \\ \hline 11110000 \end{array}$$

01
20

Q2)

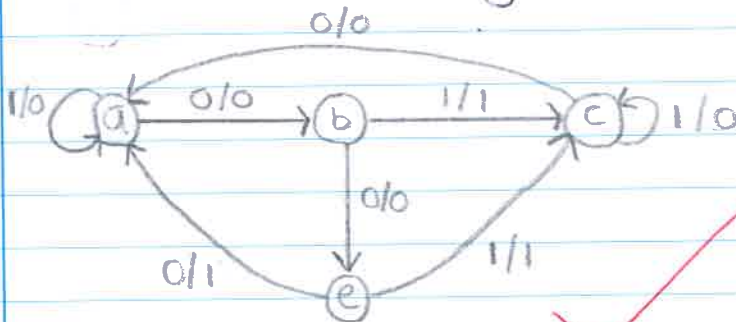
i)

PS	Next state		Output	
	x=0	x=1	x=0	x=1
a	b	d	0	0
b	e	c	0	1
c	d	c	0	0
d	b	d	0	0
e	a	c	1	1

Replace d with a

PS	Next state		Output	
	x=0	x=1	x=0	x=1
a	b	a	0	0
b	e	c	0	1
c	a	c	0	0
e	a	c	1	1

Reduced state diagram



Q2)

ii) State Assignments

- a) $a \rightarrow 00$
 $b \rightarrow 01$
 $c \rightarrow 10$
 $e \rightarrow 11$

b)

	$y_1 y_0$	Input	Next state	Output
	PS	X		
a	00	0	01	0
	00	1	00	0
b	01	0	11	0
	01	1	10	1
c	10	0	00	0
	10	1	10	0
e	11	0	00	1
	11	1	10	1

c)

	$y_1 y_0$	X	Next state	D_1	D_0	output
	PS			$\bar{D}_1$		Z
	00	0	01	0	1	0
	00	1	00	0	0	0
	01	0	11	1	1	0
	01	1	10	1	0	1
	10	0	00	0	0	0
	10	1	10	1	0	0
	11	0	00	0	0	1
	11	1	10	1	0	1

d) K-maps

D_1

$x \backslash y_1 y_0$	00	01	11	10
0		1	1	
1		1		1

$D_1 = \bar{y}_1 y_0 + \bar{x} y_0 + x y_1 \bar{y}_0$

D_0

$x \backslash y_1 y_0$	00	01	11	10
0	1	1		
1				

$D_0 = \bar{x} \bar{y}_1$

$$Z$$

$x \backslash y_1 y_0$	00	01	11	10
0			1	
1		1	1	

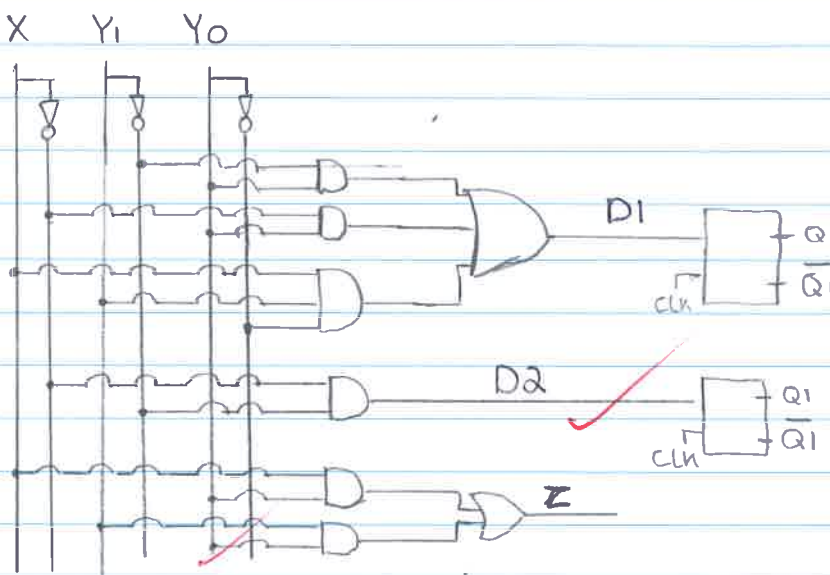
$$Z = XY_0 + Y_1 Y_0$$

$$D_1 = \bar{Y}_1 Y_0 + \bar{X} Y_0 + X Y_1 \bar{Y}_0$$

$$D_2 = \bar{X} \bar{Y}_1$$

$$Z = X Y_0 + Y_1 Y_0$$

e)

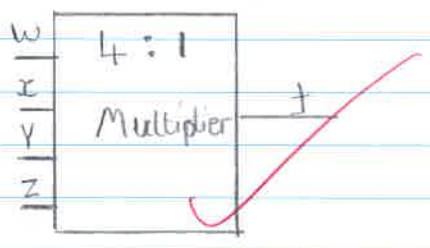


2

16/20

Q2 = 16

Q1)



2

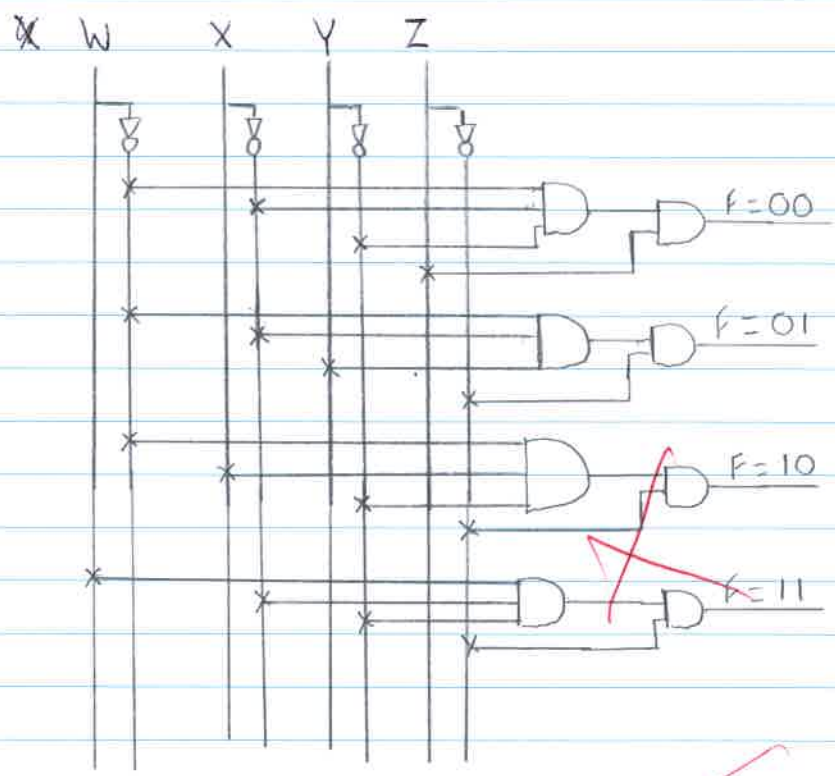
b) Truth table

Ans

W	X	Y	Z	F_{01}	F
0	0	0	1	00	Z
0	0	1	0	01	Y
0	1	0	0	10	X
1	0	0	0	11	W

1

c)



0

03
20

3

Q1