

2024888

by Ethan Rigby

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Module: SGEE4003 - Electronics1
Assignment Title: Assignment 2 - Digital Circuit Design
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University number: 2024888
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60-65

- ① RESEARCH WAS OK, BUT WRITTEN IN REVERSE ORDER
CITATIONS WERE CORRECT FORMAT, BUT YOU
COULD EXPAND THE RANGE OF SOURCES.
- ② DESIGN WAS REASONABLY WELL EXPLAINED, BUT
YOU NEEDED TO SHOW THE K-MAP GROUPS.
- ③ TESTING WAS CARRIED OUT, FINAL SYSTEM
COULD HAVE BEEN MORE COMPREHENSIVE.
- ④ SOME ANALYSIS OF RESULTS AND BRIEF CONCLUSIONS.

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State table



present state	Next state	present			next		
		QA	QB	QC	QA+	QB+	QC+
S0	S1	0	0	0	0	0	1
S1	S2	0	0	1	0	1	0
S2	S3	0	1	0	0	1	1
S3	S4	0	1	1	1	0	0
S4	S5	1	0	0	1	0	1
S5	S0	1	0	1	0	0	0
S6	X	1	1	0	X	X	X
S7	X	1	1	1	X	X	X

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2. Introduction, aims and objectives.

This assignment builds and analyses a digital counting circuit in order to understand how to read a binary sequence and convert it into logic functions. The aim is to create a digital counter that counts from 0-59 and resets itself back to 0 on a continuous loop when one external clock is added. the circuit will be monitored and tested ensuring that every aspect of the counter works how it should and that the binary is in the right order shown by logic analysers.

Aim = WHAT.
Objective = How.

3. Research

FPGA's

A Field Programmable Gate Arrays (FPGA's) are semiconductor integrated circuits consisting of a large volume of logic gates and flip flops, separated into Configurable Logic Boxes (CLB's) (Martinez, 2018). the CLB's are interconnected to create specific circuits for desired functions. These CLB's can be edited to reconfigure the function of the circuit on 'field', meaning it can be reconfigured at home, in office or on site. Unlike microcontrollers FPGAs are reconfigured through hardware, but, instead of physically changing connections they are programmable interconnections. This means that when the circuit needs to be edited it can be reconfigured using Hardware Description Languages (HDL's) such as 'Verilog and 'VHOL'. FPGAs are also getting reconfigured using High-Level Synthesis (HLS) which is programmed in subset C which is then transformed into correct Verilog code (Martinez, 2018). Due to the Flexibility and powerful applications of FPGA's they are widely used in a variety of situations such as in Aerospace, Automotive, Broadcasting, Data centres and high-level computer data storage systems (XILINX, 2021). Due to this board not being pre-built for their purpose by manufacturers FPGAs are sold off the shelf making them quick to receive (they will just require reconfiguring when received.) (intel, 2021) A diagram showing an FPGA circuit is found in 'figure 1'.

ASIC's

An Application Specific Integrated Circuit (ASIC) is an integrated circuit that is designed to handle a specific function. Unlike the FPGA these circuits are non-standardised circuits typically used for large production applications. The ASIC circuit is made up from logic functions traditionally, more recently they have started being created with analogues, these are called mixed signal ASICs. (electronicnotes, 2021) this means that they can be used for applications such as mobile phones where the analogue side is needed. Mobile phones are also ideal users of these boards as they produce the most efficiency into the smallest circuit possible. ASICs are especially useful in systems due to the overall systems electronics all being in one place as the board will provide the user with

mostly all the components needed for the specification required. There are typically 3 levels of ASICs, these levels being: -

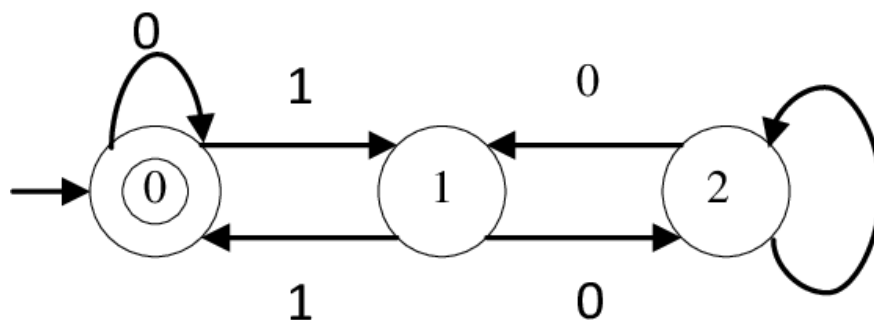
Gate array- this is the least customisable ASIC that will supply a large volume of logic functions specifically connected for the desired function of the circuit.

Standard cell- these are pre-designed logic/flip flop cells that are created into a library to create functions such as multipliers and memory arrays.

Full custom design- these circuits are made specific for the exact function required. It used logic functions mostly in customizable cells, a microprocessor is an example of a full custom ASIC where it will use every space possible to make the circuitry as small but as efficient as possible.

Finite State machine (FSM)

A finite state machine is a sequential circuit that takes pre-set sequenced logic and shows it in an orderly form. An FSM will use a low volume of potential states that need to be applied in a certain order for the next state to continue. (electronics-club, 2020) An example of this is a toll gate, a coin must be inserted into the gate in order for an alarm to sound and the gate to open, when one vehicle passes through the sequence needs to occur again to open the gates and sound the alarm a second time.



The FSM is used for more basic circuits due to its lack of complexity. But due to its simplicity it does make logic more easily visible and explainable with its visual aid and easy to understand order of events. Finite state machines can be composed by blocks of small circuits that are connected to provide a final result, so logic gates and timers can create a circuit that will act on the next block in line until the necessary outputs activate the final result.

Difference between combinational and sequential logic

The main difference between both is the components in which the circuits have. Combinational logic circuits only consist of logic functions, meanwhile sequential logic composes of logic and memory elements. Due to these two differences, it also changes the way the outputs work on both circuits. Combinational logic outputs only act dependant on the current situation of the logic, unlike the sequential where it will rely on the current logic and any previous logic states that have occurred (electronicscoach, 2021). Due to the sequential logic circuit having memory bits it also needs to have a feedback loops in order for the memory bits to function in the circuit. An example of combinational logic would be an encoder while an example of sequential logic would be the finite state machine.

RESEARCH TOPICS ARE IN REVERSE ORDER.

4. Design method

7 segment starters

In the finite state machine, there is a need for 2, 7 segment starter circuits to defuse the logic created in the previous circuits to function the LEDs in the correct order. A truth table is created to show the binary numbers needed to control the 7-segment counter. 15 different numbers were used with only 10 needed for the system to function but the others are present as they are needed in the Karnaugh maps. In all the steps below a state table is created, this shows the binary number at the current state and the next state, these tables are used to create a Karnaugh map. The Karnaugh map is used to transpose the binary numbers into a Boolean equation, this equation will be used to create a logic circuits that will be used to create the timing circuits.

inputs				outputs						
A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	1	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1
1	0	1	0	X	x	X	x	X	x	X
1	0	1	1	X	X	X	X	X	X	X
1	1	0	0	X	X	X	X	X	X	X
1	1	0	1	X	X	X	X	X	X	X
1	1	1	0	X	X	X	X	X	X	X
1	1	1	1	x	X	x	X	X	X	x

Karnaugh maps/Boolean equations for each LED segment

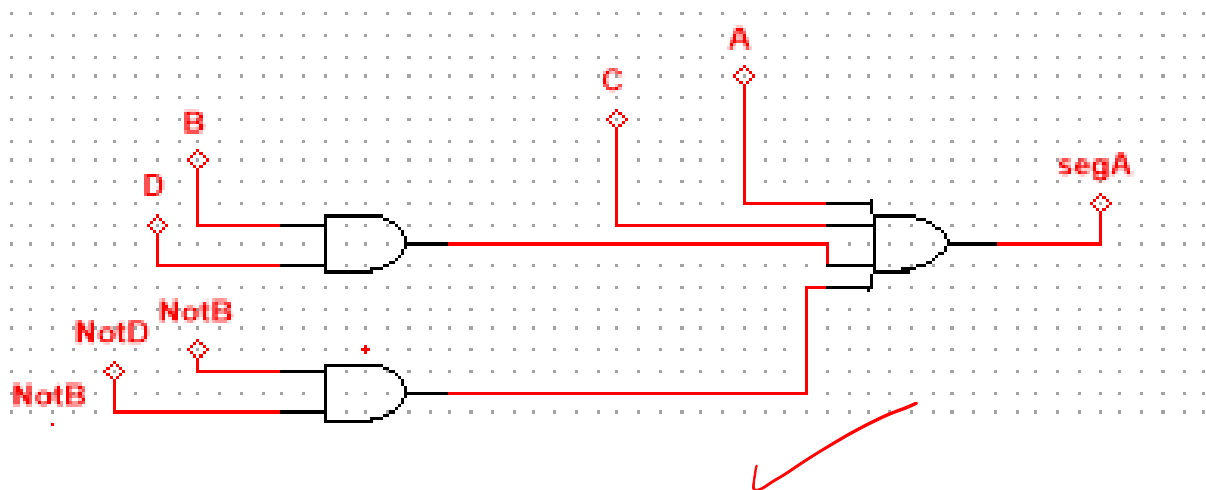
a

each of these maps creates a Boolean equation.

a	CD				
AB		00	01	11	10
	00	1	0	1	1
	01	0	1	1	1
	11	X1	X1	X1	X1
	10	1	1	X1	X1

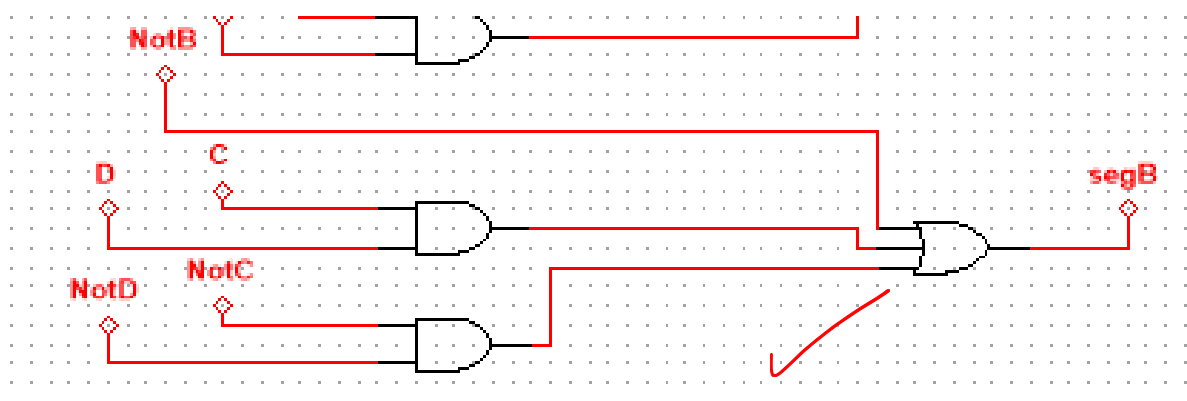
Equation= $A + C + BD + \overline{BD}$

*SOME WAY OF SHOWING
THE GROUPS IS NEEDED*



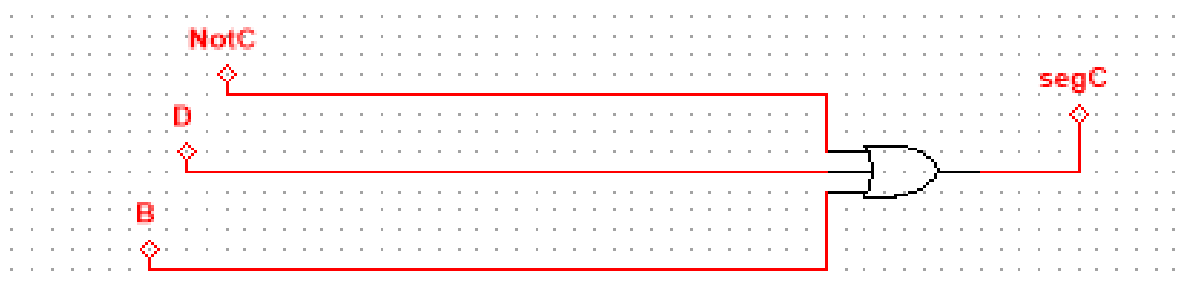
b	CD				
AB		00	01	11	10
	00	1	1	1	1
	01	1	0	1	0
	11	X1	x	X1	X
	10	1	1	X1	X1

$$\text{Equation} = \overline{B} + CD + \overline{CD}$$



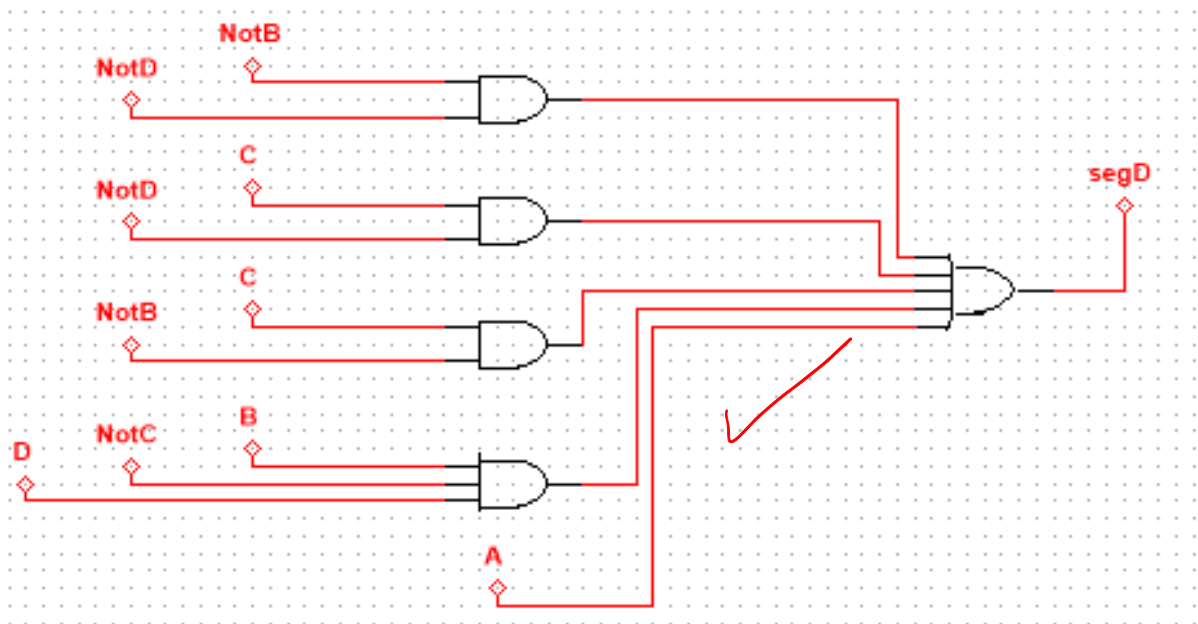
c	CD				
AB		00	01	11	10
	00	1	1	1	0
	01	1	1	1	1
	11	X1	X1	X1	X1
	10	1	1	X1	x

$$\text{Equation} = \overline{C} + \overline{AD} + B$$



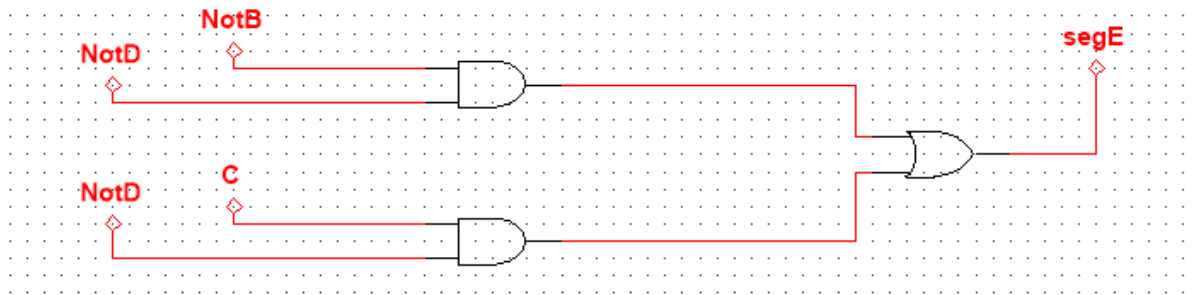
d	CD				
AB		00	01	11	10
	00	1	0	1	1
	01	0	1	0	1
	11	X1	X1	X1	X1
	10	1	1	X1	X1

Example= $\overline{B}D + \overline{B}CD + A + \overline{C}D + \overline{C}B$



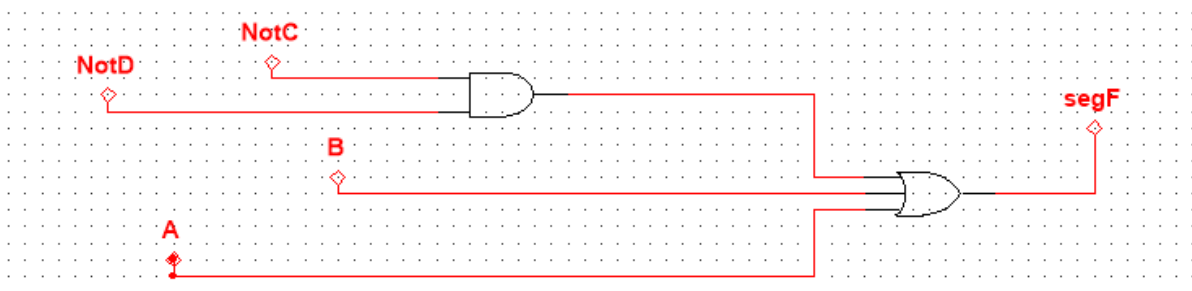
e	CD				
AB		00	01	11	10
	00	1	0	0	1
	01	0	0	0	1
	11	x	x	x	X1
	10	1	0	x	X1

$$\text{Equation} = \overline{BD} + \overline{CD}$$



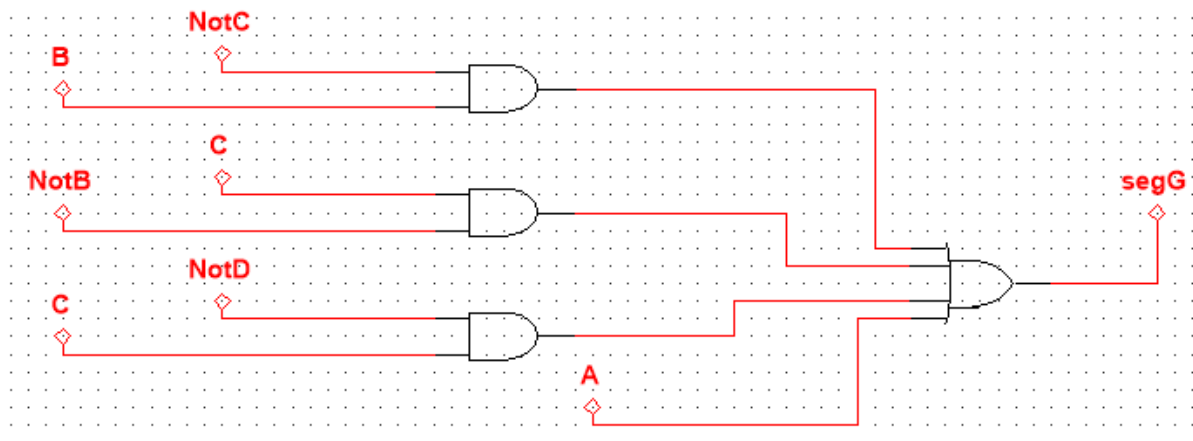
f	CD				
AB		00	01	11	10
	00	1	0	0	0
	01	1	1	1	1
	11	X1	X1	X1	X1
	10	1	1	X1	X1

$$\text{Equation} = \overline{CD} + B + A$$



g	CD				
AB		00	01	11	10
	00	0	0	1	1
	01	1	1	0	1
	11	X1	X1	X1	X1
	10	1	1	X1	X1

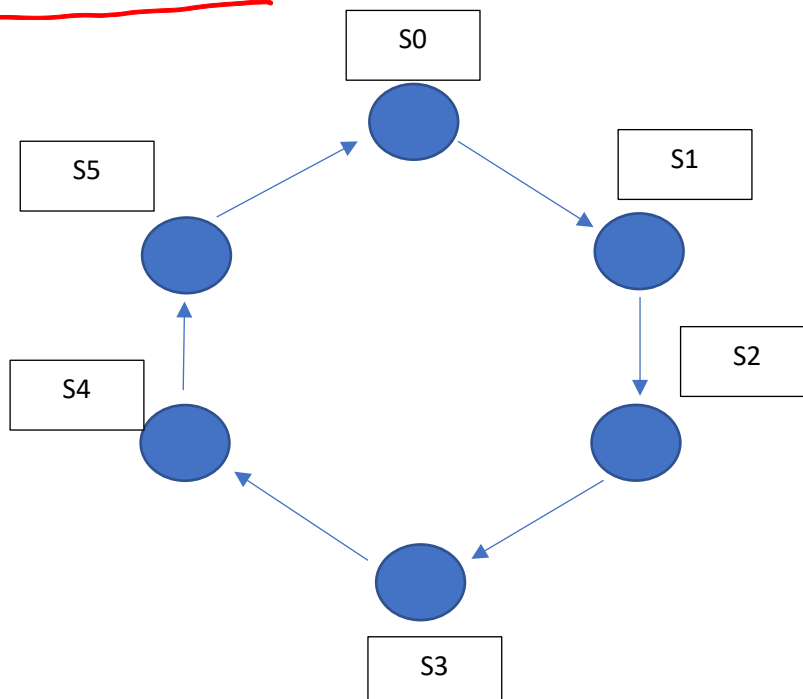
$$\text{Equation} = \bar{C}B + A + C\bar{B} + CD$$



5 second counter

Within the counting circuits there are flip flops that is connected to the logic and to a clock that is externally provided, the flip flops take the two inputs and create the output that goes to the 7-segment starter circuits. There is also a 'NOT' variant of the output that for the not logics that are used in the input.

→ STATE ALLOCATION.



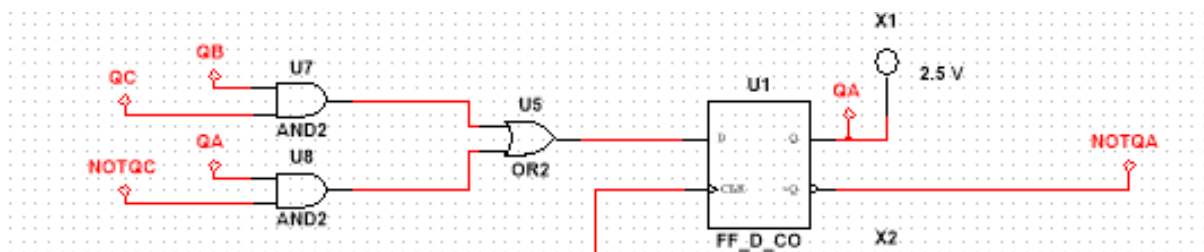
State table

present state	Next state	present			next		
		QA	QB	QC	QA+	QB+	QC+
S0	S1	0	0	0	0	0	1
S1	S2	0	0	1	0	1	0
S2	S3	0	1	0	0	1	1
S3	S4	0	1	1	1	0	0
S4	S5	1	0	0	1	0	1
S5	S0	1	0	1	0	0	0
S6	X	1	1	0	X	X	X
S7	X	1	1	1	X	X	X

Karnaugh maps/Boolean equations

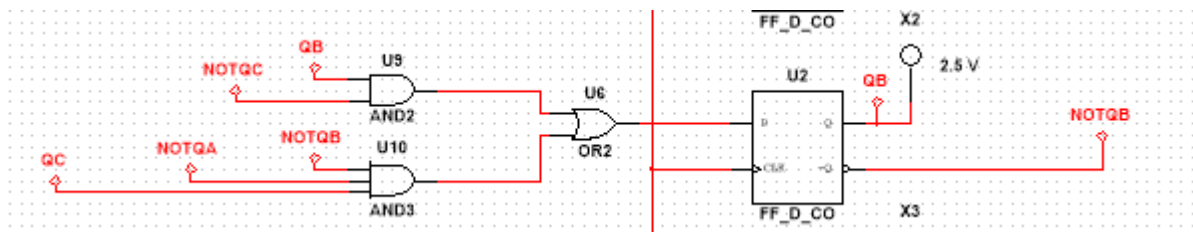
QA+	QBQC				
QA		00	01	11	10
	0	0	0	1	0
	1	1	0	X1	X1

$$\text{Equation} = QBQC + QA\overline{QC}$$



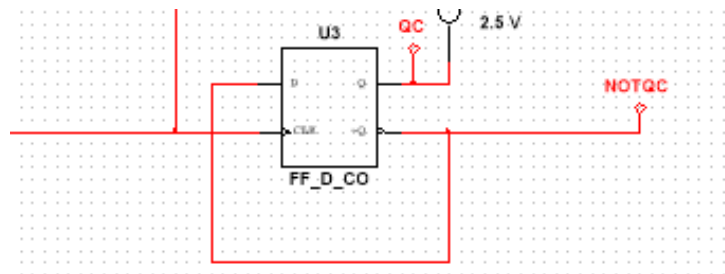
QB+	QBQC				
QA		00	01	11	10
	0	0	1	0	1
	1	0	0	X1	X1

Equation= QBQC + QAQBQC



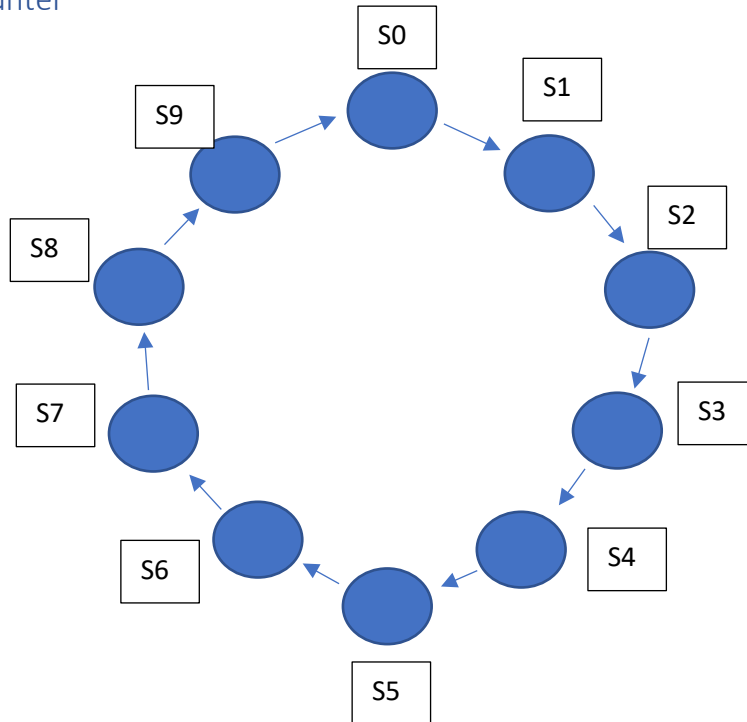
QC+	QBQC				
QA		00	01	11	10
	0	1	0	0	1
	1	1	0	X	X1

Equation= QC



STATE ALLOCATION.

Decade counter



State table

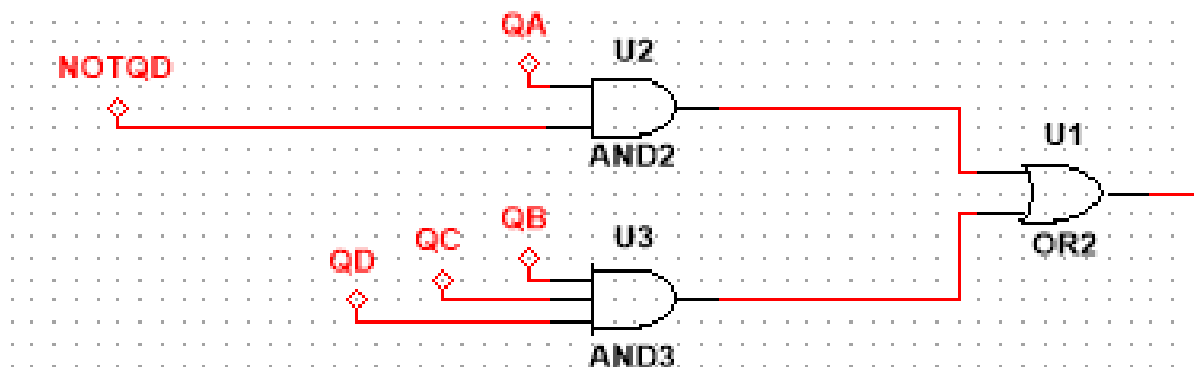
		current				next			
current	next	QA	QB	QC	QD	QA+	QB+	QC+	QD+
S0	S1	0	0	0	0	0	0	0	1
S1	S2	0	0	0	1	0	0	1	0
S2	S3	0	0	1	0	0	0	1	1
S3	S4	0	0	1	1	0	1	0	0
S4	S5	0	1	0	0	0	1	0	1
S5	S6	0	1	0	1	0	1	1	0
S6	S7	0	1	1	0	0	1	1	1
S7	S8	0	1	1	1	1	0	0	0
S8	S9	1	0	0	0	1	0	0	1
S9	S0	1	0	0	1	0	0	0	0
S10	X	1	0	1	0	X	X	X	X
S11	X	1	0	1	1	X	X	X	X
S12	X	1	1	0	0	X	X	X	X
S13	X	1	1	0	1	X	X	X	X
S14	X	1	1	1	0	X	X	X	X
S15	X	1	1	1	1	X	X	X	X



Karnaugh maps/Boolean expression

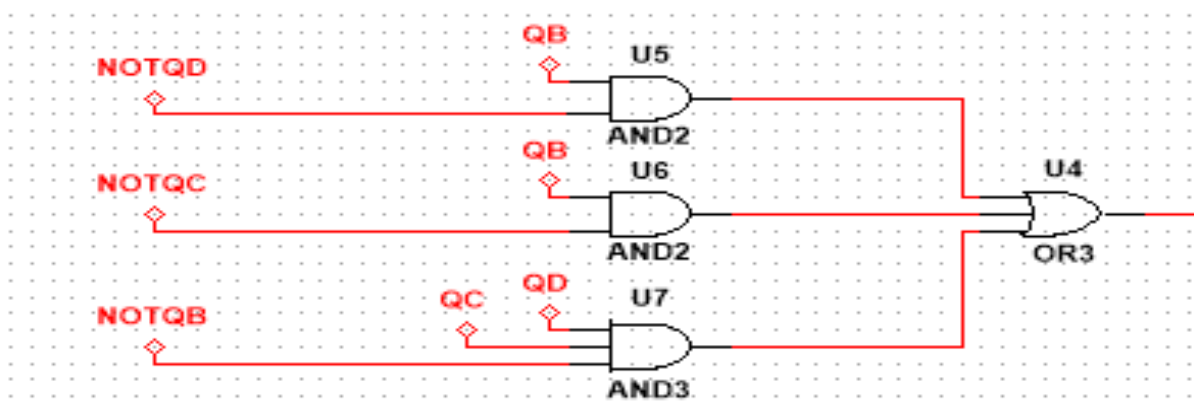
QA+	QCQD				
QAQB		00	01	11	10
	00	0	0	0	0
	01	0	0	1	0
	11	X1	X	X1	X1
	10	1	0	X	X1

Equation= QAQD + QBQCQD



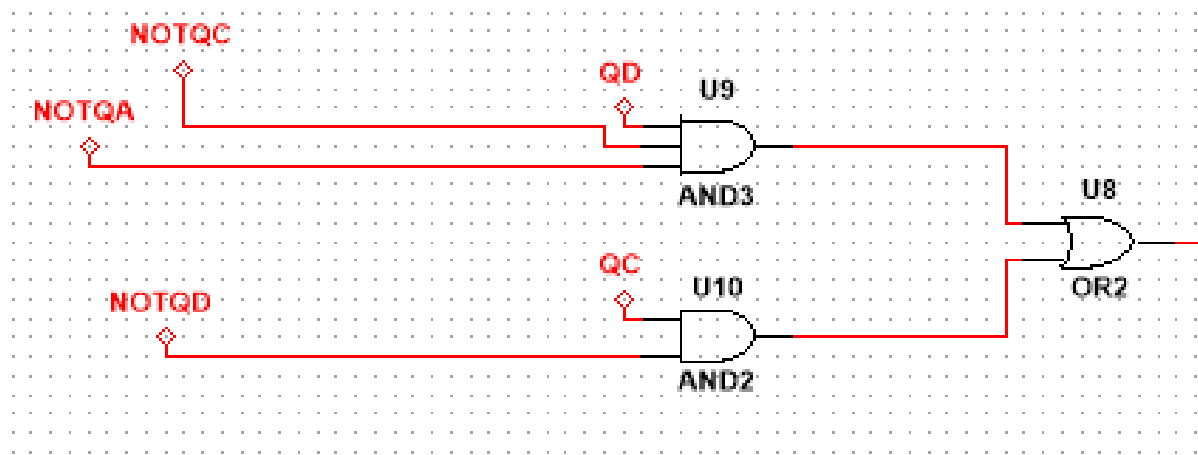
QB+	QCQD				
QAQB		00	01	11	10
	00	0	0	1	0
	01	1	1	0	1
	11	X1	X1	X	X1
	10	0	0	X1	X

Equation= $\overline{QBQD} + \overline{QBQC} + \overline{QBQCQD}$



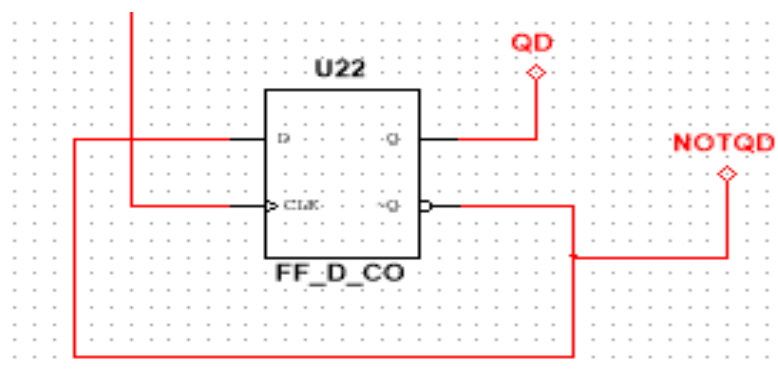
QC+	QCQD				
QAQB		00	01	11	10
	00	0	1	0	1
	01	0	1	0	1
	11	X	X	X	X1
	10	0	0	X	X1

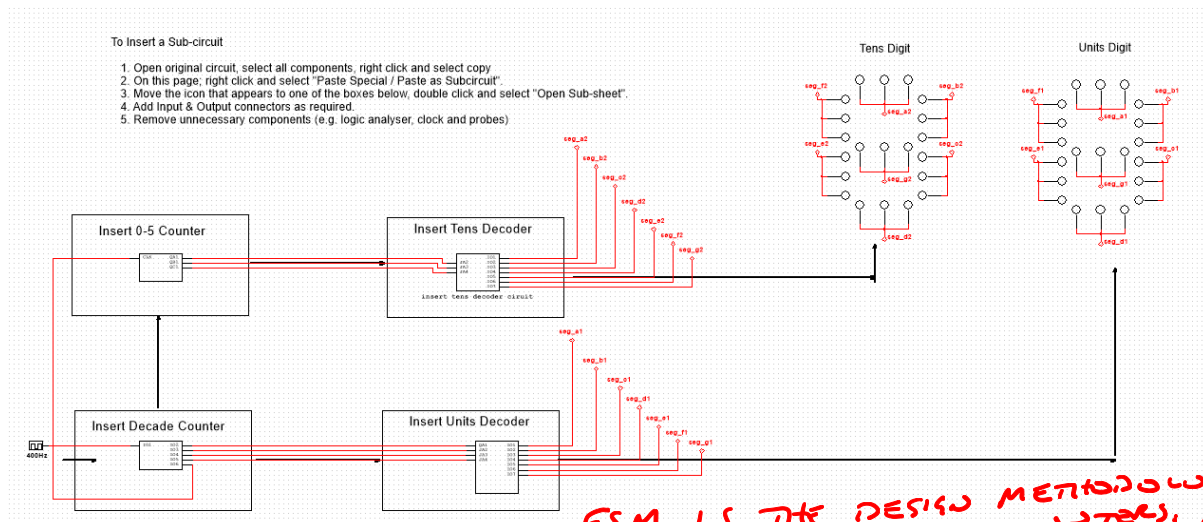
$$\text{Equation} = QAQCQD + QC\overline{QD}$$



QD+	QCQD				
QAQB		00	01	11	10
	00	1	0	0	1
	01	1	0	0	1
	11	X1	X	X	X1
	10	1	0	X	X1

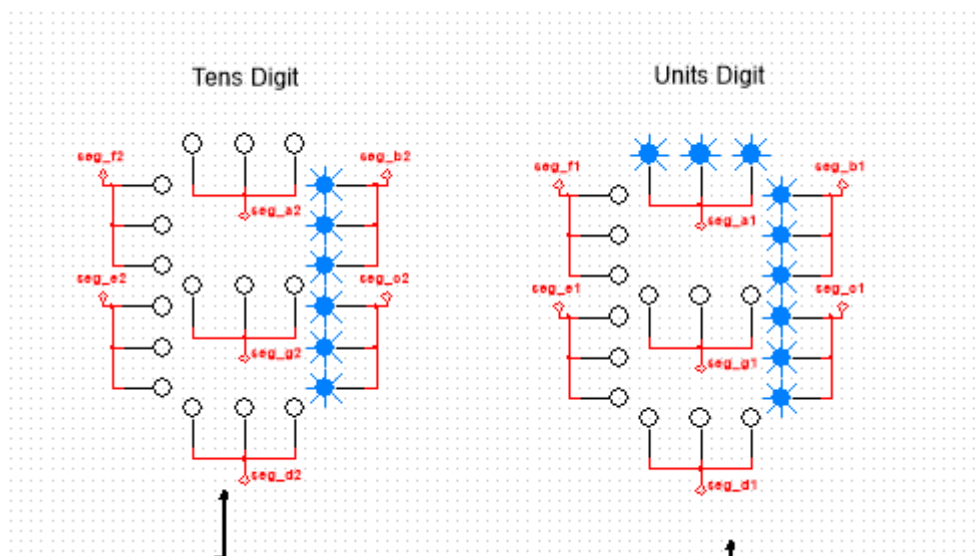
$$\text{Equation} = \overline{QD}$$





FSM IS THE DESIGN METHODOLOGY FOR EASY OF THE COUNTER, NOT THE SYSTEM

The 3 circuits were compressed into an FSM system where the inputs and outputs were all interlinked so that the resultant of the function in one circuit activated the circuit after it which would result in the tens 7-segment display adding one value for every 9 seconds that the unit digit displayed.



5. Analysis of results

Decade counter

Using a logic analyser, the outputs from the decade counter can be connected and the analyser shows the logic gates in action with the binary numbers viably shown from 0000 to 1001. This is shown in 'figure 2' and the means of connection is shown in 'figure 3'. By reading the logic analyser the binary sequence in order can be read, if compared to the state table then the sequence number at that current time can be seen.

5 second counter

Much like the decade counter the 5 second counter was also connected to a logic analyser via the outputs from the flip flops. Due to this system needing fewer flip flops than the decade counter, the binary values go from 000 to 101. By looking at the logic analyser and comparing the sequence of the binary numbers to the state table the current sequence number is visible. If the sequences move from the lowest value to the highest value and repeat themselves then the logic circuit is correct. The logic analyser and circuit are in 'figure 4' and 'figure 5'.

7-segment starter

On the 7-segment starter circuit a 7-segment display was linked up to the outputs of each logic function, each output controlled a separate function of the display. When simulating the inputs in the correct order the 7-segment display screen would count from 0-9, this is what they are needed for, they will convert the counting circuit from the decade counter and the 5 second counter and convert it into numbers in the display screen. Examples of the 7-segment starter are shown in 'figure 6'.

6. Conclusions

As seen by the results of the simulations its visible that creating a repeating counting circuit is possible with the use of logic circuits and flip flops. We can also see that the use of combinational and sequential logic can be used together to form the circuit. From looking at the design of the counter its seen that the segment starter circuit is combinational logic with the use of only logic circuits used. The circuit shows that the output from the counting circuits cause the segment starter to work and activate the segment display. The sequential logic used in the counting circuits included memory flip flops. These circuits were created with the knowledge of what the next binary conditions were going to be.

YOU COULD HAVE CONCLUDED THE DIFFERENCES BETWEEN SEQUENTIAL AND COMBINATIONAL CIRCUITS IN A LOT MORE DETAIL.

7. Reference list and bibliography

References

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[Accessed 21 March 2021].

LIST IS OK, BUT MOST OF YOUR RESEARCH
ONLY USED THE FIRST 3 ENTRIES.

8. Annexe for supplementary diagrams, data sheets and large results tables etc.

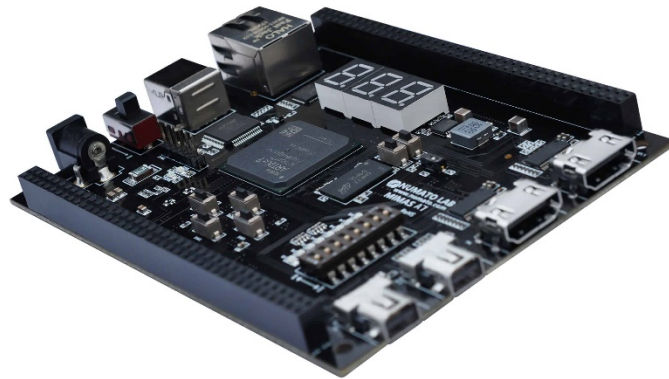


Figure 1//FPGA circuit

(Martinez, 2018)

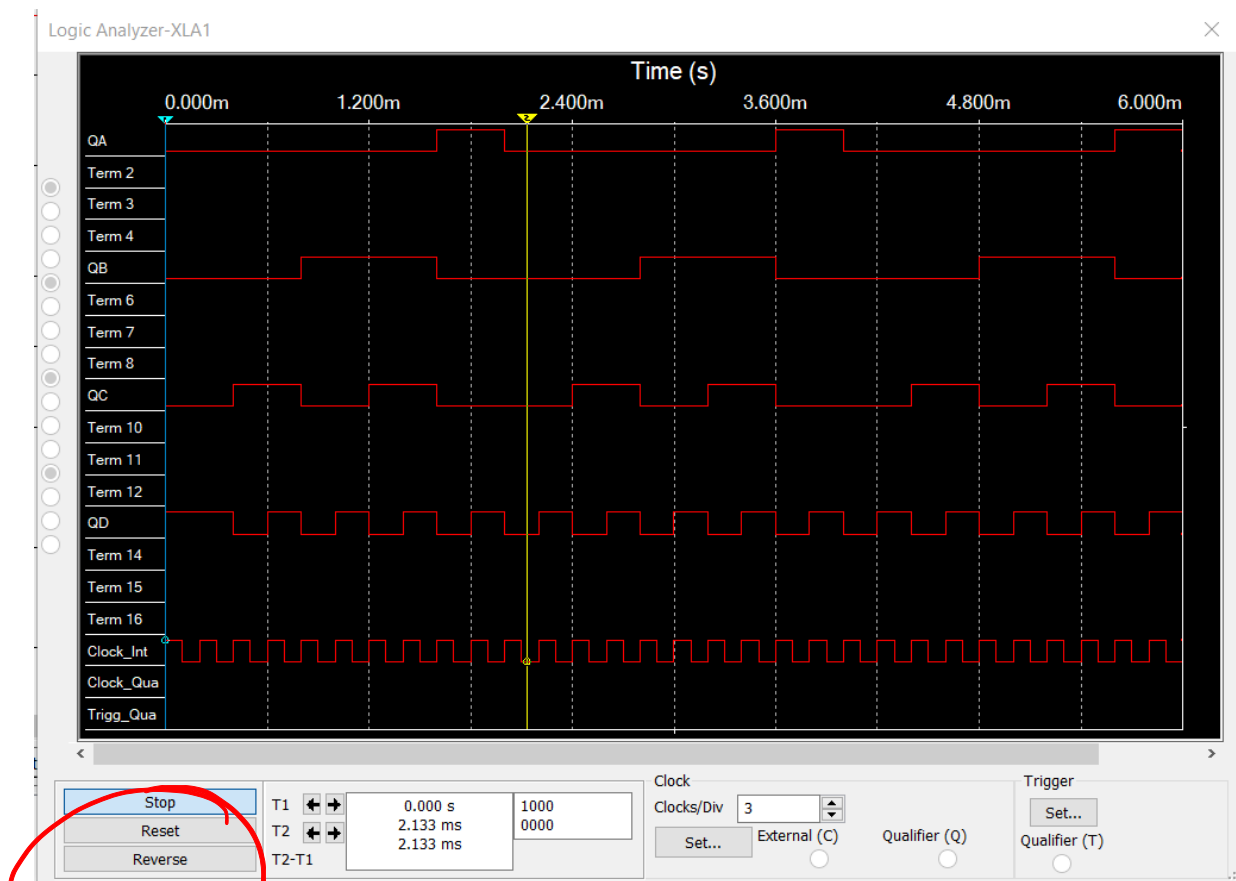


Figure 2//decade counter circuit analysis

USE REVERSE FOR
A WHITE SCREEN.

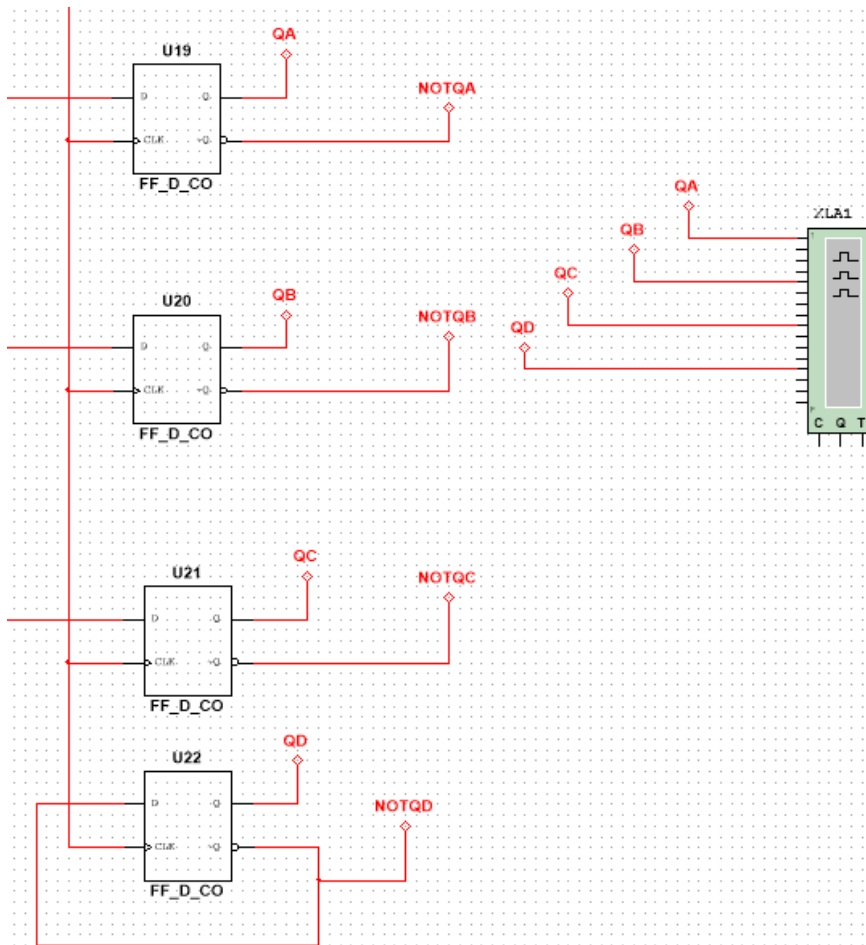


Figure 3//decode circuit

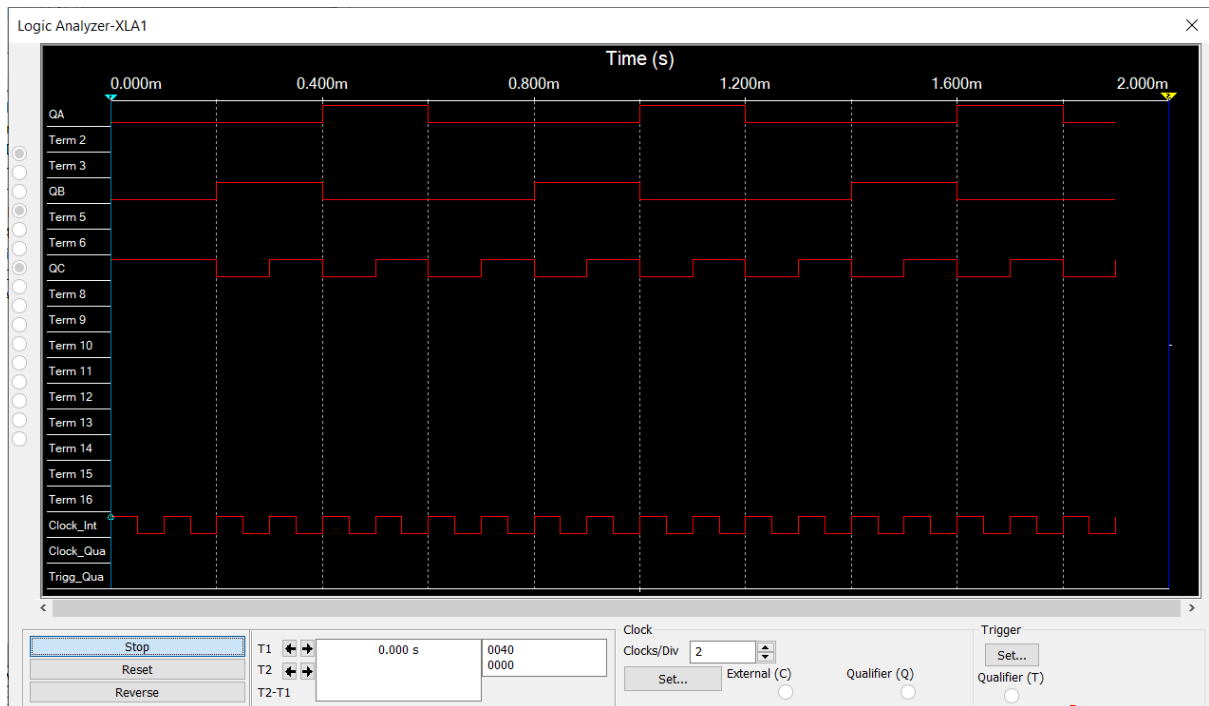


Figure 4//5 second counter

THESE GRAPHS COULD HAVE BEEN PUT IN THE BODY OF THE REPORT.

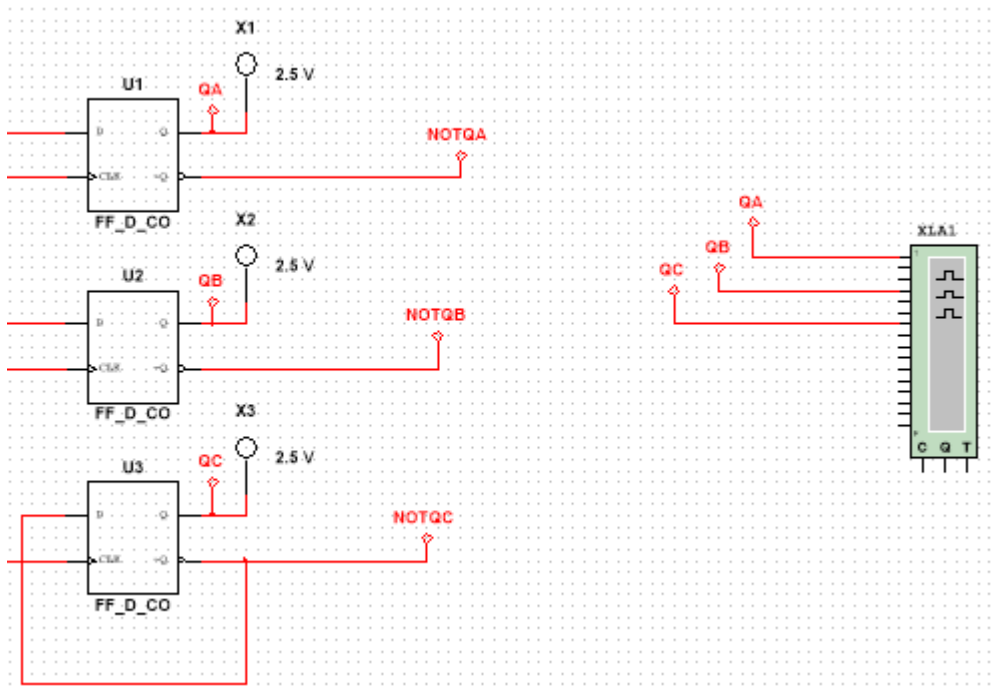


Figure 5//5 second counter

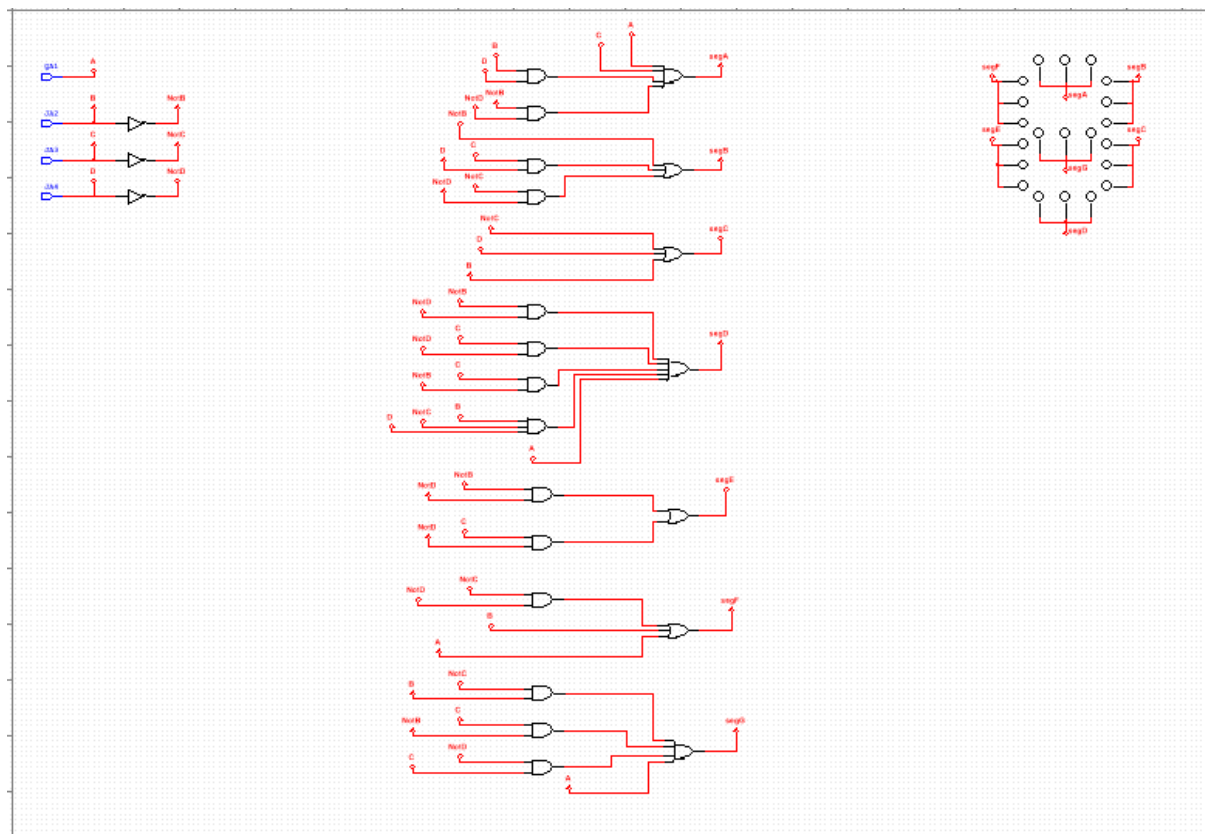


Figure 6//7-segment starter circuit

FINAL GRADE

GENERAL COMMENTS

Instructor

61 / 100

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GRADING FORM: CSG-RUBIC

ETHAN RIGBY

0

RESEARCH-INFORMED LITERATURE



There was evidence of further reading and research with the inclusion of a reference list and appropriate in text referencing. Your interpretation and understanding of the additional research was good. Your references were appropriate to the task and your reference list was of an appropriate length for this assignment. Some of the sources were over-used and you should consider widening your range of sources for future assignments.

6/10

KNOWLEDGE AND UNDERSTANDING



The knowledge and understanding of the subject demonstrated by this assignment was reasonably extensive. There were very few gaps in your knowledge of the basic principles and your understanding of the higher level concepts was demonstrated to a limited degree. You have demonstrated some critical understanding of the main concepts and expanded your knowledge beyond that contained in the course notes, however your explanations need to be more detailed and written with a greater emphasis on critical evaluation rather than description.

19/30

ANALYSIS



Your explanation of the design process was good and the conclusions showed that you can interpret quantitative and qualitative data, although this was often descriptive. You could have evaluated the results and specified whether they concurred with theory suggesting reasons for any discrepancies. You have however demonstrated good analytical skills and your approach to the task was logical. Arguments made in the conclusions were mostly valid and demonstrated a good understanding of the topic. Further work – in your conclusion, you should relate the results to the original specification and to accepted theory.

16/30

PRACTICAL APPLICATION AND DEP.



Your application of practical skills for this task was generally adequate. You used the resources appropriately when designing the circuit and you

13/20

used appropriate options for testing and evaluating the circuit performance. You managed to design a basic circuit that functioned within the specification and achieved this by only asking for assistance when appropriate thus demonstrating some basic problem solving skills. Your results were adequate and allowed for a reasonable conclusion to be attempted.

SKILLS FOR PROFESSIONAL PRAC.



In this assignment you have demonstrated skills in working individually and also collaboratively. Your written report was written in a professional and confident style, however you still need to be more efficient with your word count. The report was very well presented, with excellent diagrams in appropriate places, good sentence/paragraph structure and clear calculations.

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