

2024423

by Taylor Hoskins

FILE	16348_TAYLOR_HOSKINS_2024423_179157_1222469813.PDF (1,003.64K)		
TIME SUBMITTED	03-MAY-2021 05:20PM (UTC+0100)	WORD COUNT	3820
SUBMISSION ID	151447348	CHARACTER COUNT	17011

Course: HNC Electrical and Electronic Engineering
Module: SGEE4003 - Electronics1
Assignment Title: Assignment 2 - Digital Circuit Design
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University number: 2024423
Date Submitted: 03/05/2021
Word Count: 2737 words

70-75

- ① GOOD RESEARCH AND CORRECTLY FORMATTED CITATIONS.
GOOD RANGE OF SOURCES.
- ② DESIGN METHOD WAS EXPLAINED IN DETAIL AND
IN A LOGICAL ORDER.
- ③ COMPREHENSIVE TESTING WAS EVIDENT, BUT THE LOGIC
ANALYSER WASN'T ALWAYS SET TO ITS OPTIMAL
SETTINGS.
- ④ VERY GOOD ANALYSIS OF THE RESULTS.
- ⑤ SOME REASONABLE CONCLUSIONS, ALWAYS USE 3RD PERSON
THOUGH.

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1. Executive Summary

The project involved creating a stopwatch testbed which was able to count from 0-59 repeatedly. This was done by creating a 0-5 counter, 0-9-decade counter and a decoder on Multisim. All were added as subcircuits into a test sheet and connected through on page connectors. Research was carried out about combination and sequential logic circuits, including uses of flipflops. It was decided sequential logic circuits would best suit this task. A full set of tests were carried out on all circuits using Logic Analysers and light probes. The specification was met but there was an issue with the final circuit where it started on the value eleven.

*THIS SHOULD COVER ALL SECTIONS
OF THE REPORT.*

2. Introduction, aims and objectives.

A stopwatch testbed which counts from 0-59 repeatedly is made up of subcircuits using sequential logic. They contain AND, OR and NOT gates, as well as flipflops for the circuit to work.

The aims for this document are:

- Conduct research of Combinational and Sequential Logic Circuits
- Design a 0-59 second stopwatch testbed.
- Produce results to test the test bed
- Analyse the results thoroughly.

Aims = WHAT.
Objectives = HOW.

3. Research

In a digital circuit, there are two types of logic which can be used – Combinational and Sequential. Combinational logic is used to produce the next-state function and the output function for both synchronous and asynchronous sequential machines. The output is purely dependent on the present input as it receives no feedback. This means the change in input is the only thing that effects the output, and it can be said that Combinational logic holds no memory. The circuit use AND, OR, NOT, NOR and NAND gates in order to produce these. The input is binary and can either be logic 0 or logic 1, which will generate outputs. (Cavanagh, 2006)



FIGURE 1

(Administator, 2015)

Sequential logic works differently to combinational. It is essentially a combinational logic circuit with added memory. This memory element can store binary, which allows positive feedback of the previous output. In this logic circuit, the output is now dependent on the past output as well as the present input. A clock signal is used to send pulses to the input at regular intervals.

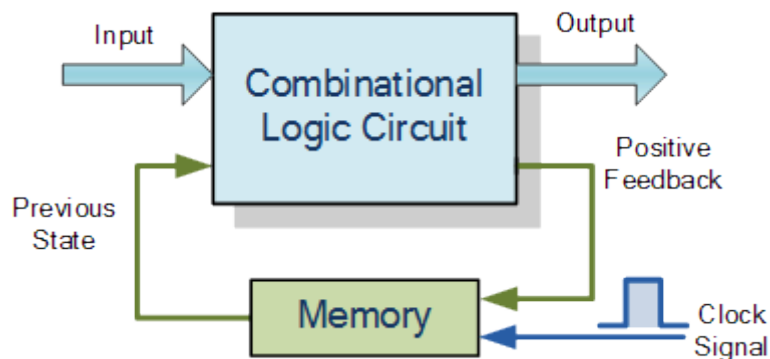


FIGURE 2

(Electronics Tutorials, 2016)

Sequential Logic can be two state of stable devices. They use states logic 0 and 1 but will 'latch' in that state until a signal is given to change the state again. Clocked flip-flops or SR latches are used in this.

An SR Latch is a basic flipflop which will either SET or RESET a device. The SET state will create a 'latch' and the reset will revert to its previous state. S and R are both inputs to the device, with Q and inverted Q being outputs. The Q output is fed back creating a Q input. The truth table for an SR latch is shown below.

S	R	Q	STATE
0	0	PREVIOUS STATE	NO CHANGE
0	1	0	RESET
1	0	1	SET
1	1	?	FORBIDDEN

FIGURE 3

(Rao, 2021)

When both S and R are equal to 1, Q is indeterminate, which could make it impractical for certain applications and JK Flipflops can be used instead.

JK Flipflops uses a clock in order to synchronise the time. They have two inputs, J and K. In a D type, the inputs are connected through an inverter so that the J and K inputs can never be the same. If J and K are different then the output Q takes the value of J at the next clock edge. There is also a T type which allows the flipflop to 'toggle'. This means that the state will change when T is equal to logic 1. The Q output can always be determined in a JK Flipflop.

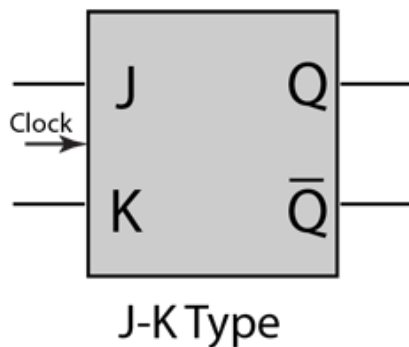


FIGURE 4

(Nave, 2019)

Finite state machines are digital circuits composed from combinational and sequential logic sections. The machine can be in a specific state from a finite set of possible states, the input can then affect the state. Sequential logic circuits can always be modelled into FSM's, but it is not always necessary. If there are too little states, then the circuit solution may be very straight forward and creating a finite state machine would be pointless. It also works the other way, where if there are too many states, then the machine may be too complex, and it can be not worth creating. With the right number of states, it can be used as an effective design pattern.

As a design tool, finite state machines can be used as a design pattern to implement software projects. They can be highly effective and can work in games, traffic control, vending machines and software where particular modes and controls are needed. They essentially accept a finite number of inputs which can produce a finite number of outputs. (Ferdinand Wagner, 2006)

"A mealy machine is defined as a machine in theory of computation whose output values are determined by both its current state and current inputs. In this machine at most one transition is possible A Moore machine is defined as a machine in theory of computation whose output values are determined only by its current state." – (Geeks for Geeks, 2020)

An FPGA is an integrated circuit. It stands for field programmable gate array and can be used to implement almost any hardware design. It is used often as a prototyping circuit, which can be implemented into an ASIC later. It consists of a two-dimensional array of logic blocks, where the function logic block, inputs and outputs and interconnections of each block can be configured. (Jean-Pierre Deschamps, 2006). FPGAs can be reprogrammed which is a massive advantage compared to other types. The user can go back into the program and change it to suit the new needs. This type is inexpensive in low numbers and therefore can be used for smaller projects.

ASICs are Application Specific Integrates circuits, which are built specifically for the given task. Once placed onto chip, they cannot be reprogrammed so can only be used for into specific purpose, rather than a general program. The advantages of this type are:

- Increased Speed

- Lower Cost for mass production
 - Low power consumption
 - Better design Security
 - Better control of I/O characteristics
 - More compact board device
- (Jean-Pierre Deschamps, 2006)

Figure 5 shows an example of an ASIC system on chip, where the software is placed onto the chip that can be hard wired in a device.



FIGURE 5

RESEARCH IS OK

4. Design method

0-5 Decade Counter

Specification

The aim of the 0-5 Decade counter is to count from 0-5 repeatedly. This will be used in the final circuit to produce the first digit.

State Allocation

- State 0 = Count 0
- State 1 = Count 1
- State 2 = Count 2
- State 3 = Count 3
- State 4 = Count 4
- State 5 = Count 5

State Diagram

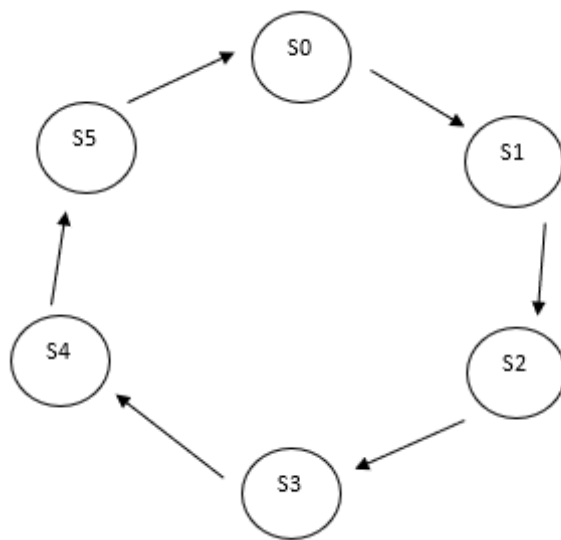


FIGURE 6

Truth Table

Present State	Next State	Current			Next		
		QA	QB	QC	QA+	QB+	QC+
S0	S1	0	0	0	0	0	1
S1	S2	0	0	1	0	1	0
S2	S3	0	1	0	0	1	1
S3	S4	0	1	1	1	0	0
S4	S5	1	0	0	1	0	1
S5	S6	1	0	1	0	0	0
S6	X	1	1	0	X	X	X
S7	X	1	1	1	X	X	X

FIGURE 7

States 0 to 5 are used in order to meet the specification. State 6 and 7 are used for a 3 flipflops to be used in a circuit. 8 states are needed, and the last two results can be used to suit the Karnaugh maps.

Karnaugh Maps

$$QA+= QB QC + QA \overline{QC}$$

	00	01	11	10
00	0	0	1	0
01	1	0	x	x

FIGURE 8

$$QB+= QB \overline{QC} + \overline{QA} \overline{QB} QC$$

	00	01	11	10
00	0	1	0	1
01	0	0	x	x

FIGURE 9

$$QC+= \overline{QC}$$

	00	01	11	10
00	1	0	0	1
01	1	0	x	x

FIGURE 10

Boolean Equations

$$QA+= QB QC + QA \overline{QC}$$

$$QB+= QB \overline{QC} + \overline{QA} \overline{QB} QC$$

$$QC+= \overline{QC}$$

These equations have been added to a digital circuit on Multisim shown in Figure 11, using AND and OR gates as well as flipflops to create a sequential logic circuit. Light probes have been added for the purpose of testing.

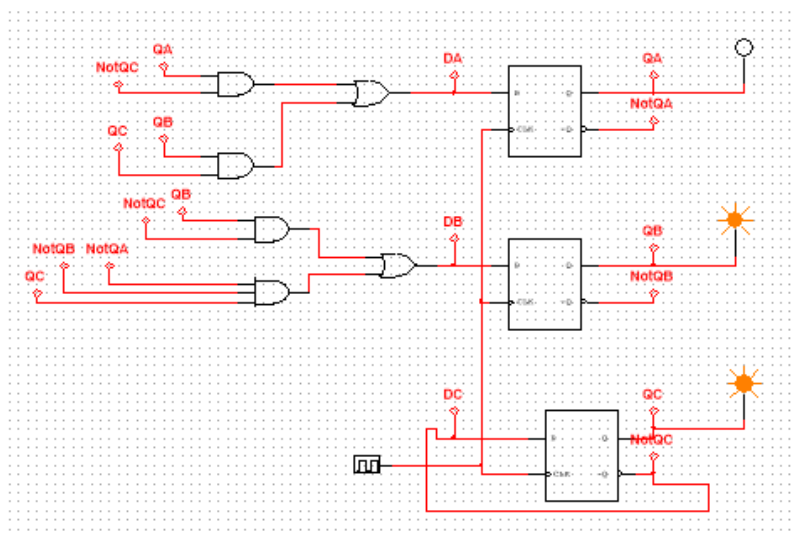


FIGURE 11

0-9 Decade Counter

Specification

The purpose of the 0-9 Decade counter is to create a circuit which can count from 0-9 repeatedly. This is connected to the Units counter in the full circuit which will control the second digit.

State Allocation

- State 0 = Count 0
- State 1 = Count 1
- State 2 = Count 2
- State 3 = Count 3
- State 4 = Count 4
- State 5 = Count 5
- State 6 = Count 6
- State 7 = Count 7
- State 8 = Count 8
- State 9 = Count 9

State Diagram

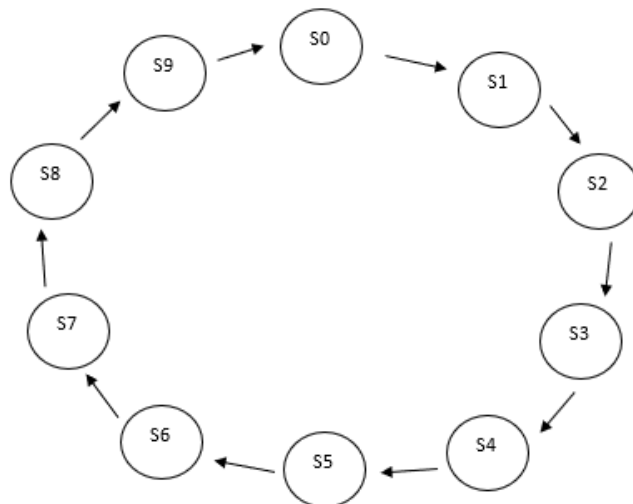


FIGURE 12

Truth Table

		Current				Next			
Current	Next	QA	QB	QC	QD	QA+	QB+	QC+	QD+
S0	S1	0	0	0	0	0	0	0	1
S1	S2	0	0	0	1	0	0	1	0
S2	S3	0	0	1	0	0	0	1	1
S3	S4	0	0	1	1	0	1	0	0
S4	S5	0	1	0	0	0	1	0	1
S5	S6	0	1	0	1	0	1	1	0
S6	S7	0	1	1	0	0	1	1	1
S7	S8	0	1	1	1	1	0	0	0
S8	S9	1	0	0	0	1	0	0	1
S9	S0	1	0	0	1	0	0	0	0
S10	X	1	0	1	0	X	X	X	X
S11	X	1	0	1	1	X	X	X	X
S12	X	1	1	0	0	X	X	X	X

S13	X	1	1	0	1	X	X	X	X
S14	X	1	1	1	0	X	X	X	X
S15	X	1	1	1	1	X	X	X	X

FIGURE 13

A 4-bit circuit requires 16 states. For the 'next' values, states 10-15 are irrelevant and therefore are used to suit the Karnaugh maps.

Karnaugh Maps

$$QA_{+} = QA \overline{QD} + QB \overline{QC} QD$$

	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	x	x	x	x
10	1	0	x	x

FIGURE 14

$$QB_{+} = QB \overline{QC} + \overline{QB} \overline{QC} QD + QB \overline{QD}$$

	00	01	11	10
00	0	0	1	0
01	1	1	0	1
11	x	x	x	x
10	0	0	x	x

FIGURE 15

$$QC_{+} = \overline{QA} \overline{QC} QD + QC \overline{QD}$$

	00	01	11	10
00	0	1	0	1
01	0	1	0	1
11	x	x	x	x
10	0	0	x	x

FIGURE 16

$$QD_{+} = \overline{QD}$$

	00	01	11	10
00	1	0	0	1
01	1	0	0	1
11	x	x	x	x
10	1	0	x	x

FIGURE 17

WELL PRESENTED.

Boolean Equations

$$QA+ = QA \overline{QD} + QB \overline{QC} QD$$

$$QB+ = QB \overline{QC} + \overline{QB} \overline{QC} QD + QB \overline{QD}$$

$$QC+ = \overline{QA} \overline{QC} QD + QC \overline{QD}$$

$$QD+ = \overline{QD}$$

A sequential logic circuit was created using the Boolean equations derived. AND, OR gates and Flipflops were used to create the 0-9 counter. Four Flipflops were required to create the circuit. It is shown below in figure 18.

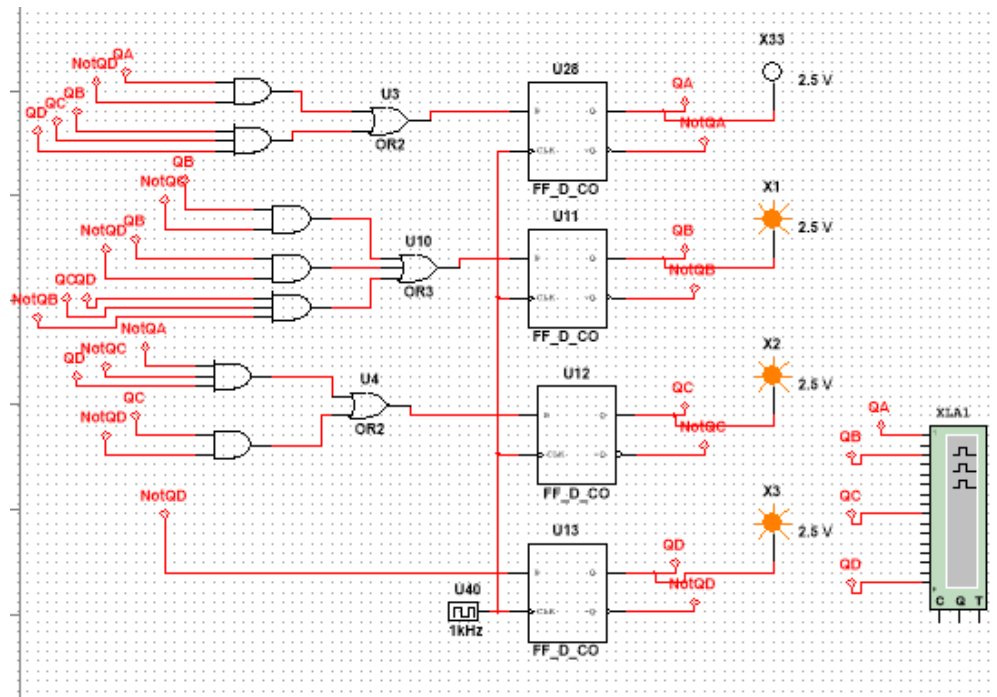


FIGURE 18

Decoder

The decoder is a 7-segment display design which allows a binary code to be converted into a display using a circuit. The circuit is made up of AND, OR and NOT gates. A truth table is created from Binary inputs which can be used to produce Karnaugh Maps. From these, equations can be derived, and a circuit can be created, producing the 7-segment display output.

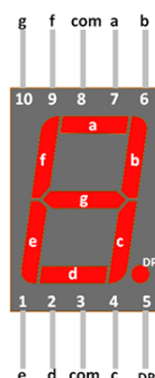


FIGURE 19

(Component 101, 2020)

Truth Table

	A	B	C	D	a	B	c	d	E	F	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	1	1
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1
A	1	0	1	0	X	X	X	X	X	X	X
B	1	0	1	1	X	X	X	X	X	X	X
C	1	1	0	0	X	X	X	X	X	X	X
D	1	1	0	1	X	X	X	X	X	X	X
E	1	1	1	0	X	X	X	X	X	X	X
F	1	1	1	1	X	X	X	X	X	X	X

FIGURE 20

Karnaugh Maps

$$a = A + C + \bar{B}\bar{D} + BD$$

	00	01	11	10
00	1	0	1	1
01	0	1	1	1
11	x	x	x	x
10	1	1	x	x

FIGURE 21

$$b = \bar{B} + \bar{C}\bar{D} + CD$$

	00	01	11	10
00	1	0	1	1
01	1	0	1	0
11	x	x	x	x
10	1	1	x	x

FIGURE 22

$$c = B + \bar{C} + D$$

	00	01	11	10
00	1	1	1	0
01	1	1	1	1
11	x	x	x	x
10	1	1	x	x

FIGURE 23

$$d = A + \overline{B}\overline{D} + C\overline{D} + \overline{B}C + B\overline{C}D$$

	00	01	11	10
00	1	0	1	1
01	0	1	0	1
11	x	x	x	x
10	1	1	x	x

FIGURE 24

$$e = \overline{B}\overline{D} + C\overline{D}$$

	00	01	11	10
00	1	0	0	1
01	0	0	0	1
11	x	x	x	x
10	1	0	x	x

FIGURE 25

$$f = A + B + \overline{C}\overline{D}$$

	00	01	11	10
00	1	0	0	0
01	1	1	1	1
11	x	x	x	x
10	1	1	x	x

FIGURE 26

$$g = A + B\overline{C} + C\overline{D} + \overline{B}C$$

	00	01	11	10
00	0	0	1	1
01	1	1	0	1
11	x	x	x	x
10	1	1	x	x

FIGURE 27

Boolean Equations

$$a = A + C + \overline{B}\overline{D} + BD$$

$$b = \overline{B} + \overline{C}\overline{D} + CD$$

$$c = B + \overline{C} + D$$

$$d = A + \overline{B}\overline{D} + C\overline{D} + \overline{B}C + B\overline{C}D$$

$$e = \overline{B}\overline{D} + C\overline{D}$$

$$f = A + B + \overline{C}\overline{D}$$

$$g = A + B\overline{C} + C\overline{D} + \overline{B}C$$

Full Circuit

The four circuits were inputted into stopwatch test bed as sub circuits with on page connectors, so that the stopwatch can count from 0-59 repeatedly. An AND gate was added to the output of the Decade counter so that the not functions would be connected to the input of the 0-5 counter. This is so it counts correctly, the first digit counts a digit every time the second digit reaches 9.

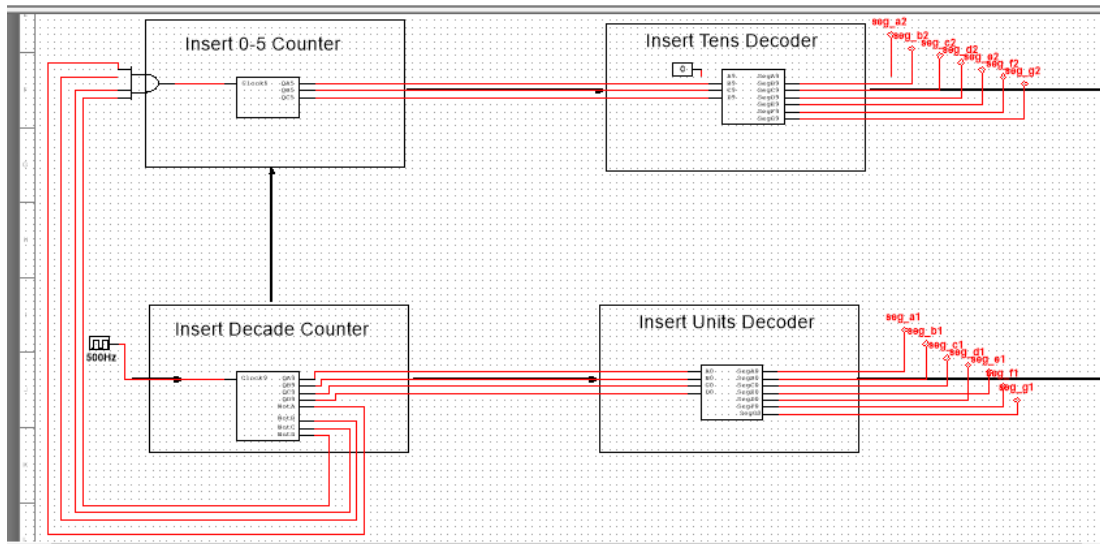


FIGURE 28

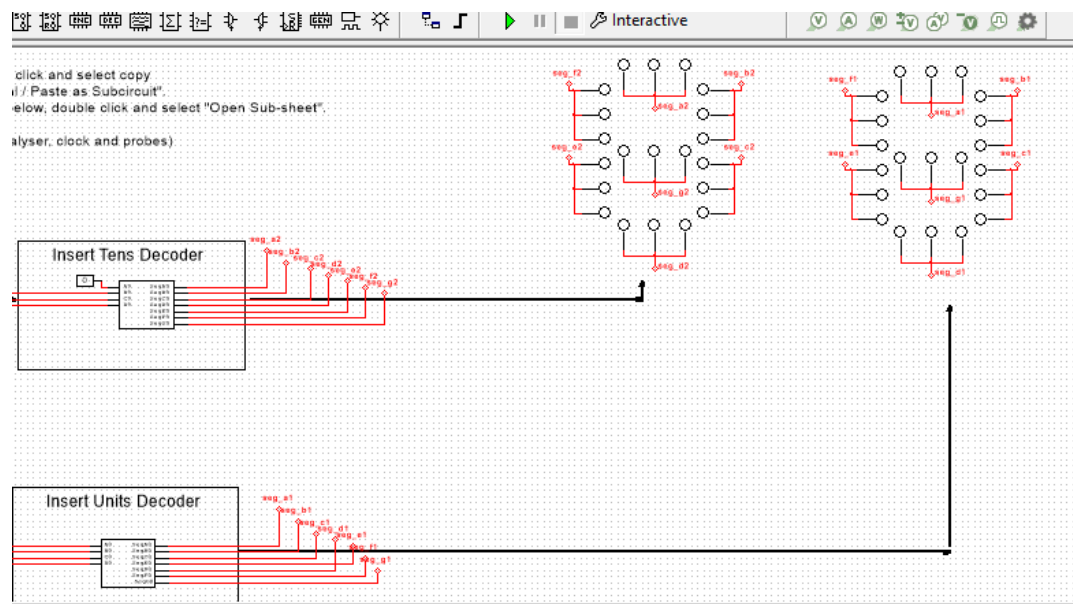


FIGURE 29

5. Analysis of results

0-5 Decade Counter

A clock is connected to the circuit flipflops to send pulses in order to test the 0-5 Decade counter. A logic analyser was used in order to show the output of QA, QB and QC. Figure 30 shows the circuit with the analyser added.

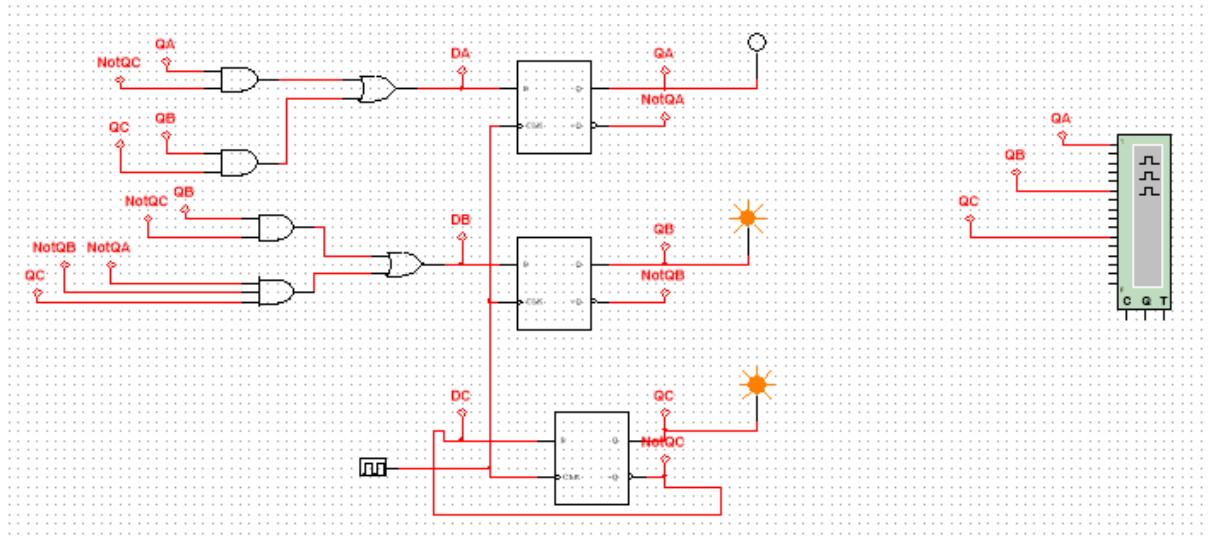


FIGURE 30

The samples and clocks have been changed to suit the logic analyser output, so that the full cycle can be shown. Each division is equal to 2 states. It can be shown on the logic analyser that when in the up state, this is equal to logic 1. The down state indicates logic 0. The probes will light when the output is equal to logic 1. Figure 31 shows the circuit State 4 as the probes for QA and QC are lit, meaning they are equal to logic 1, relating back to the truth table.

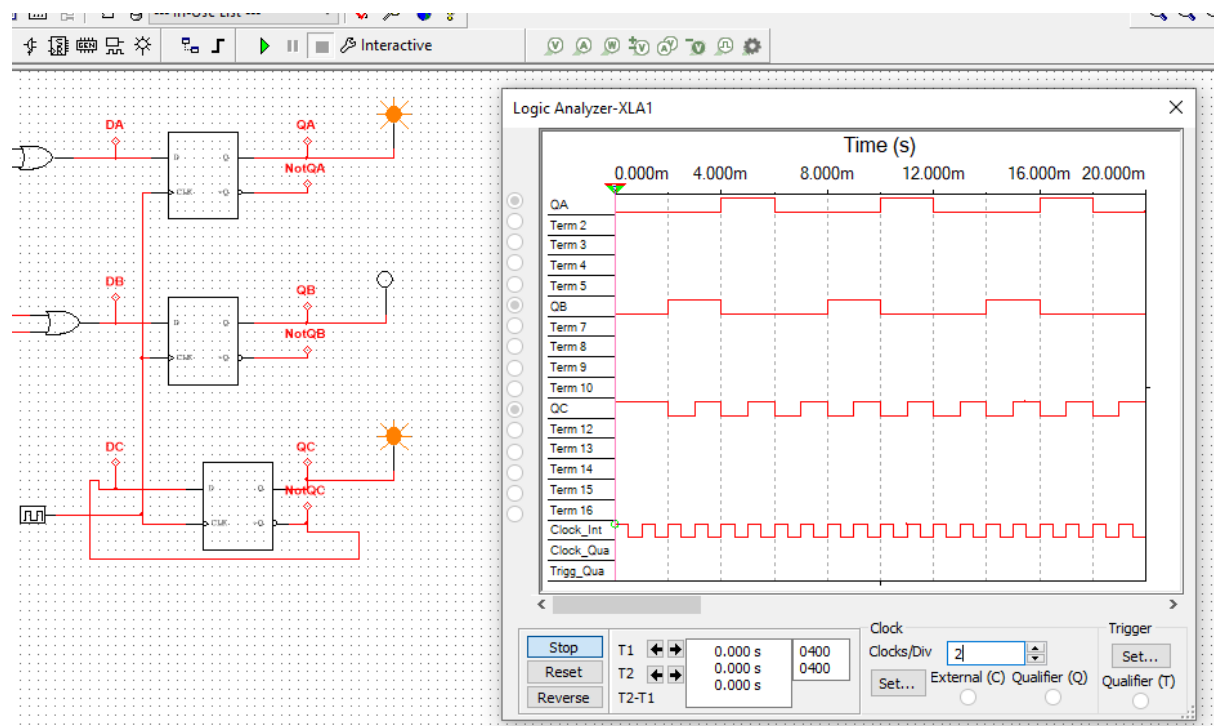


FIGURE 31

Figure 32 shows the logic analyser with added colour boxes for ease of reading each state. The yellow box shows State 0. When relating back to the truth table in figure 7, in state 0, QA and QB should be equal to logic 0 (down state) and QC should be equal to logic 1 (up state), this is shown proving that the circuit is correct. The blue box shows state 3. This is proved once again from the truth table, showing QA equal to logic 1, QB equal to logic 0 and QB also equal to logic 0. The purple box shows that the circuit is repeating correctly as it should, after state 5, the circuit should return to state 0. As there are 2 pulses per divisions, three divisions over, it should return to the same state. It proves this is working properly as this is the case, where both QA and QB are equal to logic 0 and QC is logic 0. This can now be added to the full circuit as the testing is all correct.

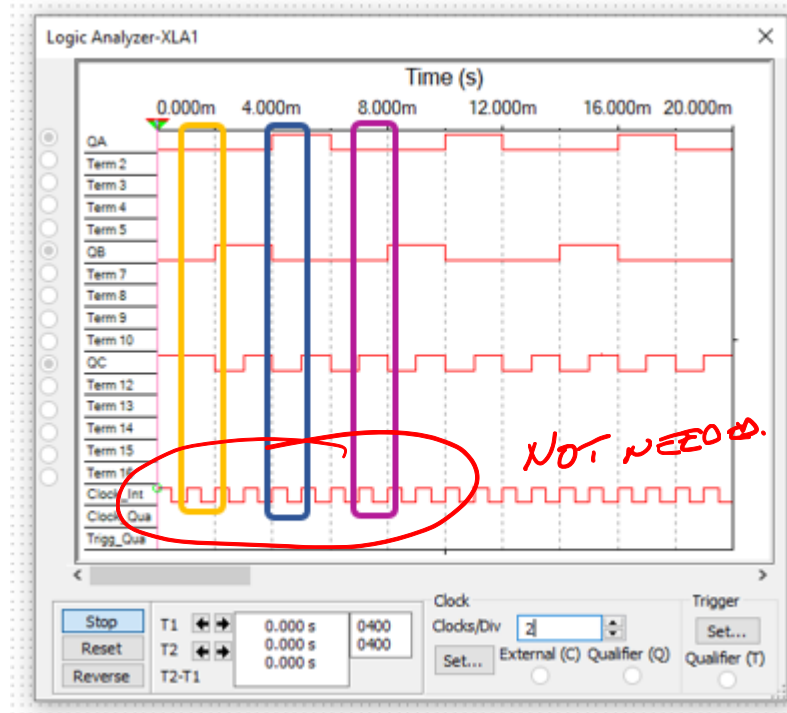


FIGURE 32

0-9 Decade Counter

The logic Analyser has also been added to the 0-9 Decade Counter in order to prove this is working. The circuit is shown with light probes attached also, when the circuit is started, if it follows the pattern of the truth table, then it can be shown the circuit is correct. For this the clock frequency is changed so that it is slowed down. Figure 33 shows a screenshot of this test in state 6. This is proved by the test table, where QA is equal to logic 0 and QB, QC and QD are equal to logic 1. Therefore, the light probes for QB, QC and QD are lit, as expected.

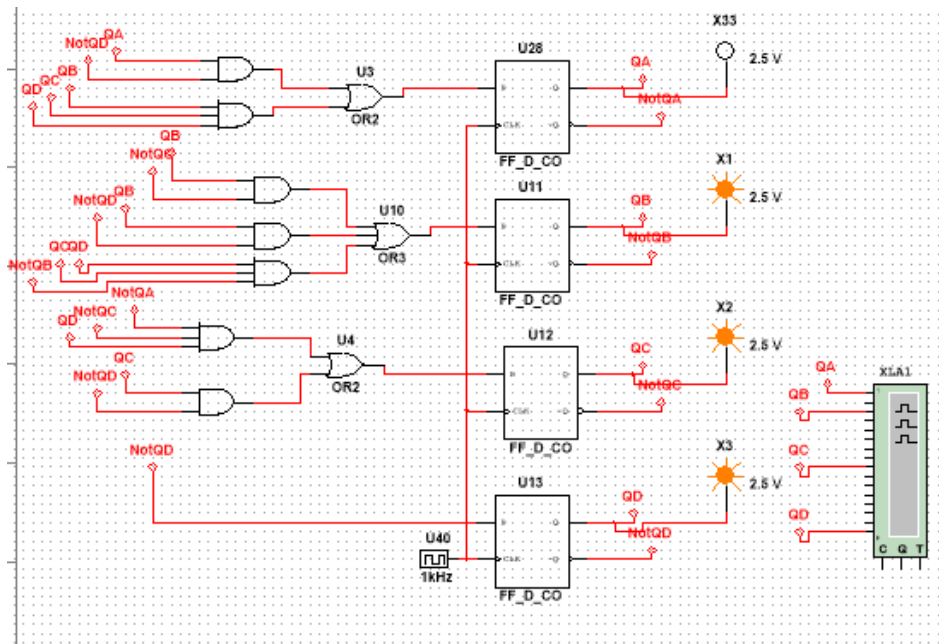


FIGURE 33

The logic analyser can better prove the sequence is correct, which is shown in figure 34. The full sequence is shown from 0 to around 10m, which will be further explored in figure 35. The blue line indicates the end of the sequence.

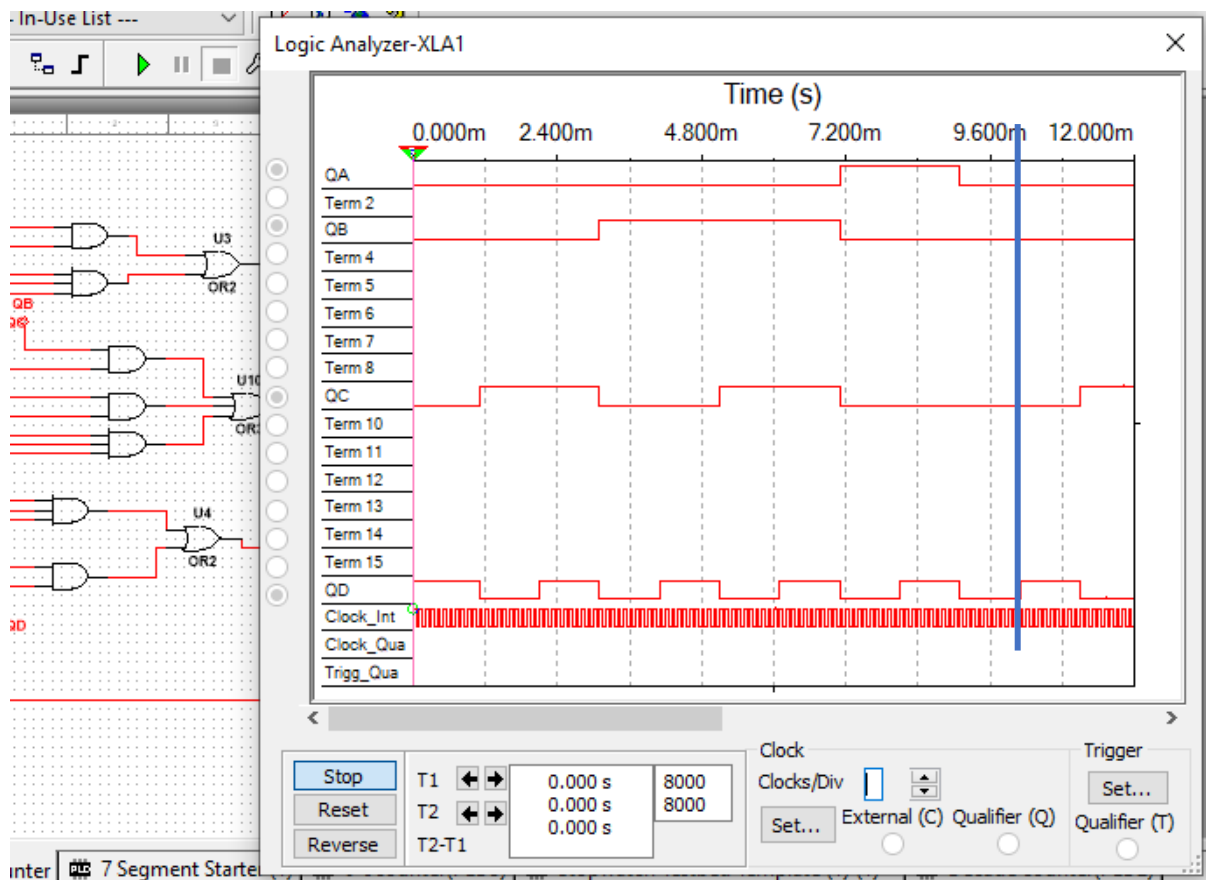


FIGURE 34

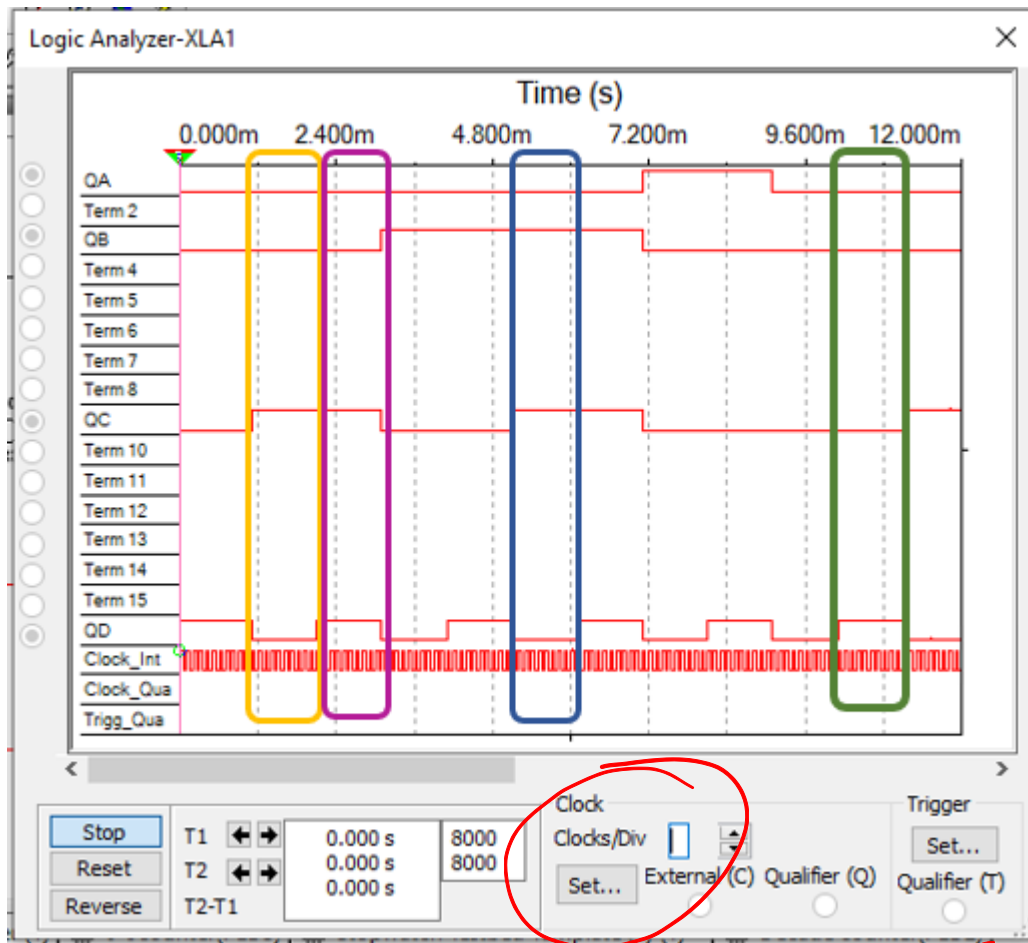


FIGURE 35

NOT SET CORRECTLY. SHOULD SHOW 20 CLOCKS, NOT 10.

Figure 35 shows the 0-9 Decade counter with coloured boxes to show a specific state. A results table has been created to compare the results against the expected.

State	Expected				Actual				PASS/ FAIL
	QA	QB	QC	QD	QA	QB	QC	QD	
S1 (Yellow)	0	0	1	0	0	0	1	0	PASS
S2 (Purple)	0	0	1	1	0	0	1	1	PASS
S5 (Blue)	0	1	1	0	0	1	1	0	PASS
S0 (Green)	0	0	0	1	0	0	0	1	PASS

FIGURE 36

The green box shows that the circuit has met its specification, repeating back to state 0 after it has counted from 0-9. All Results were as expected so the Counter is working as it should be and able to be put into the second circuit to control the second digit.

Decoder

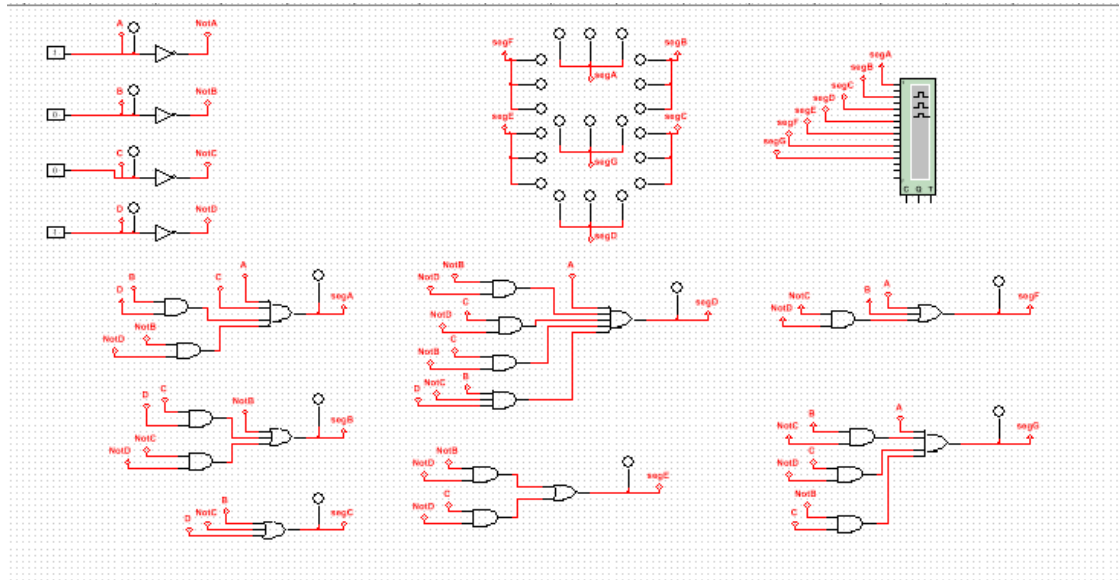


FIGURE 37

To test the decoder, a digital constant is added to A, B, C and D on page connectors. This can produce a logic 1 and logic 0 state. The segment probes will light up in accordance with the state it is in, producing the format of that number. When QA and QC are logic 0 and QB and QD are logic 1, the probes should show number 5, shown in figure 38.

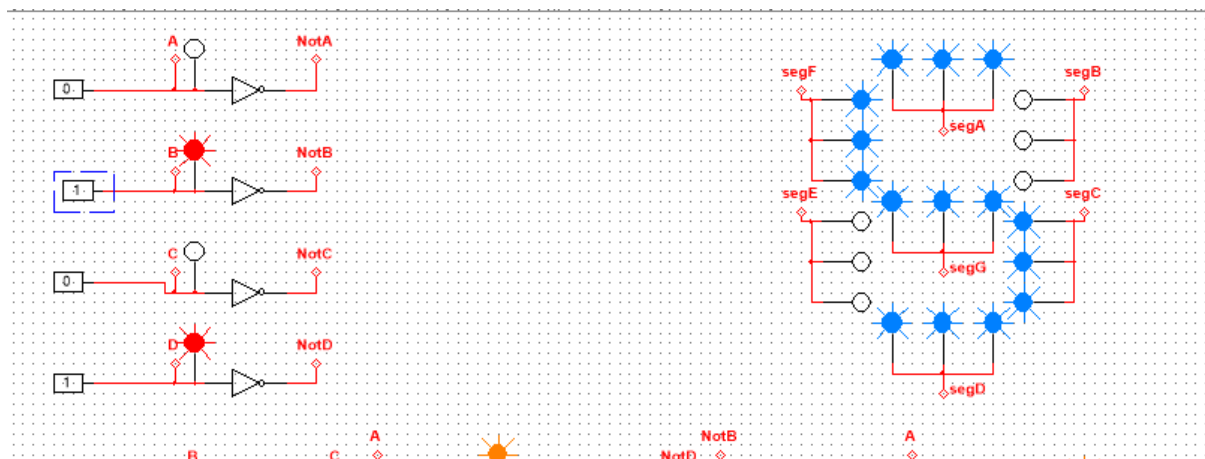


FIGURE 38

The decoder will be tested fully when added to the full circuit on the logic analyser. The logic analyser will produce a sequence once connected to the full circuit which can be tested, and the segment probes should light up in accordance with the segment states.

Full circuit

The circuits are added to the test bed as sub circuits. The clocks are removed from the Decade counters so that the full circuit can be connected, where the input clock pulse is connected to the decade counter. On page connectors are added into the sub circuits as inputs and outputs to connect the sub circuits together. On the input of the tens count, the A is not connected.

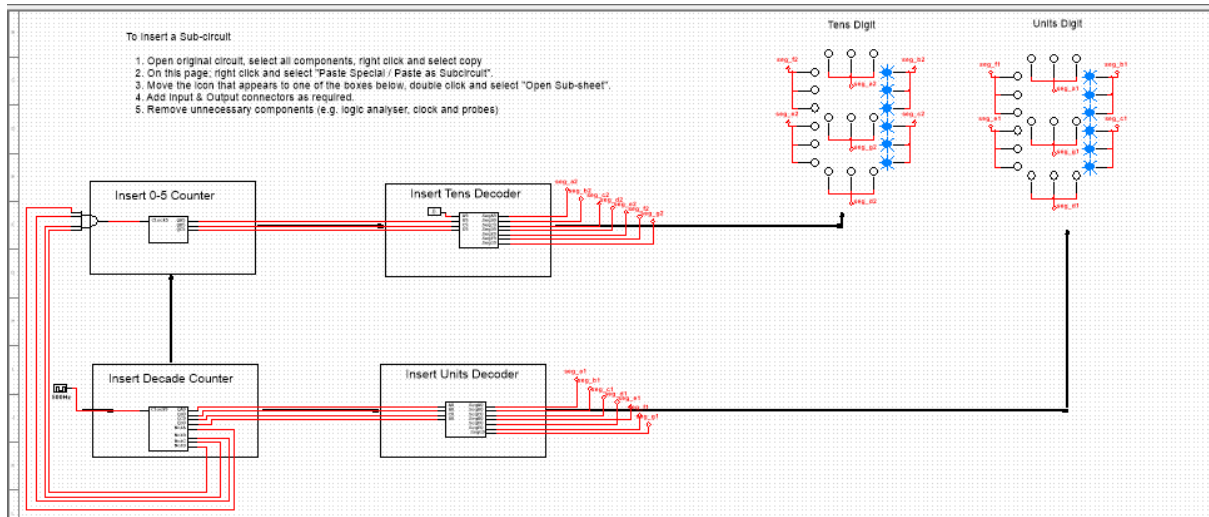


FIGURE 39

Figure 40 shows the circuit on count 42 as an example to show the circuit counting.

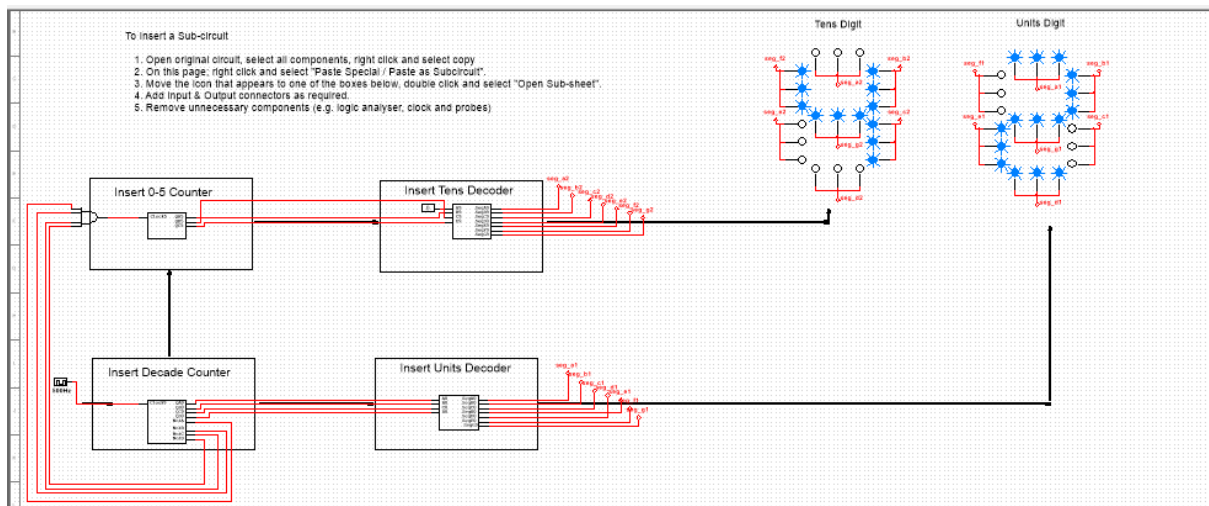


FIGURE 40

The logic analyser for the units digit for the testbed is shown below.

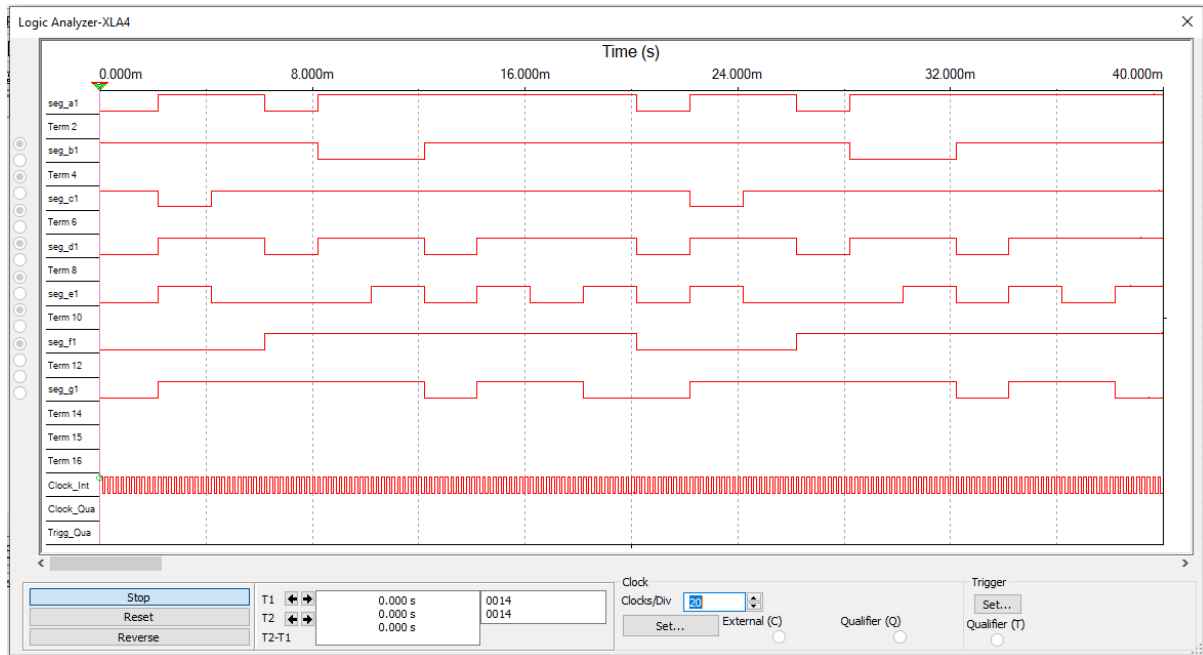


FIGURE 41

Figure 41 relates the units digit where the probes display the corresponding number to the state. The blue line indicates where the 0-9 is on repeat. After this it starts at 0 again and will continue until the circuit is stopped. The first state is state 1. Relating back to the seven-segment truth table, the purple box should follow the sequence 0110000, which is shown in figure 42. The blue box shows the sequence for state 5, the green for state 0 and yellow is the second sequence for state 5, relates back to figure 38 for comparison with the truth table.

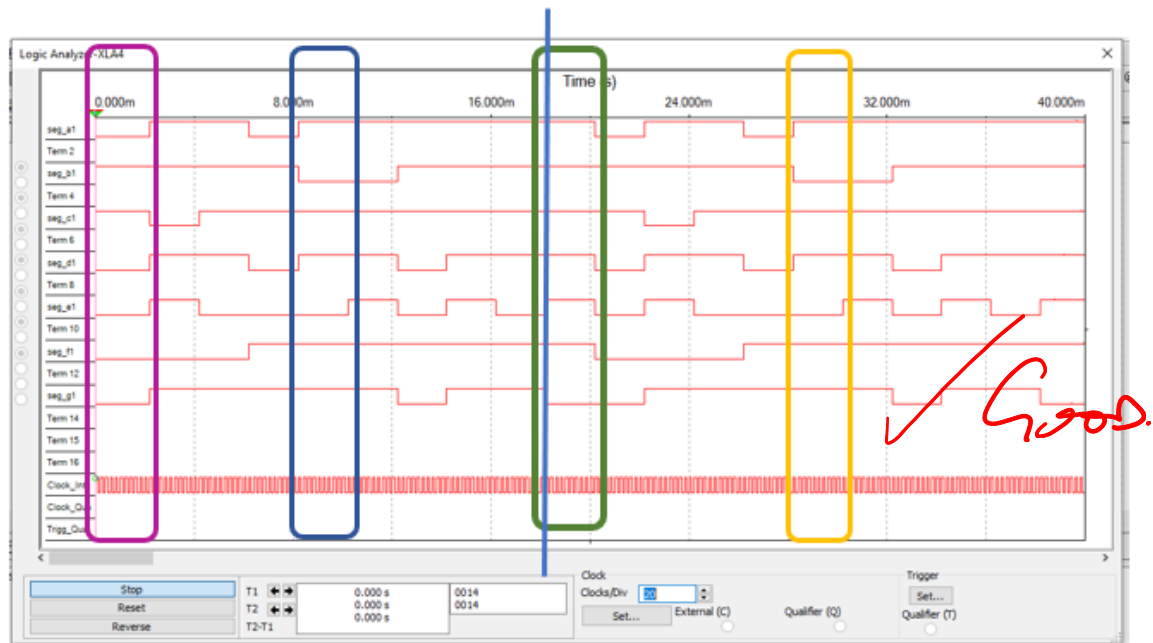


FIGURE 42

The logic analyser for the tens unit is shown in the figure 43, where all six states can be found. Starting with state 1.

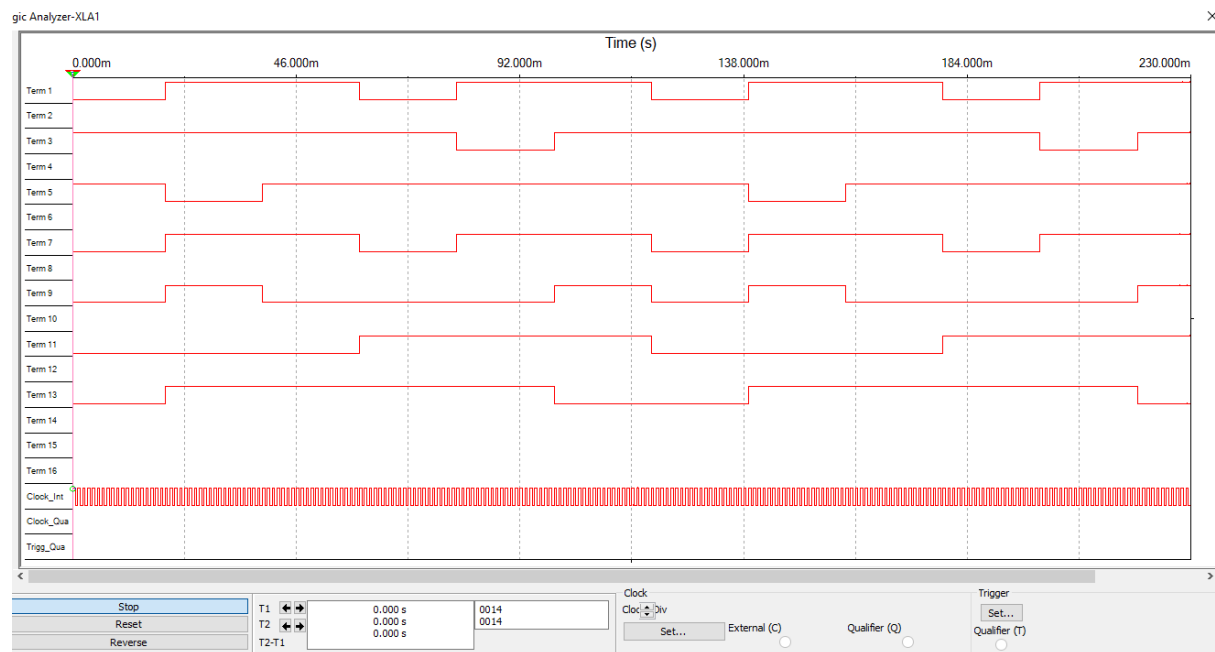
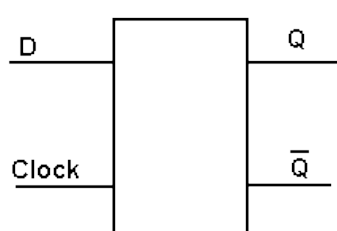


FIGURE 43

6. Conclusions

From the results, it is shown that the testbed circuit does meet the required task as the specification is to 'count from 0-59 repeatedly.' This is done by combining four circuits with on page connectors to the main testbed circuit. The logic analysers and light probes produced exactly the results that were expected and related back to the test tables and Karnaugh maps, confirming the design was correct. Figures 32, 35 and 42 show the logic analyser, with coloured boxes referring to states it was in, in the cycle.

The 0-5-decade counter and the 0-9-decade counter both were able to meet the requirements of the task. They are both sequential logic circuits. From the research, it is evident that this type needed to be used in order to count in sequence, meaning that the value must be dependent on the previous output. For example, the output of five must come after four, otherwise the circuit would not count properly. Combinational logic circuits would be unable to produce the counters as they store no memory. It was decided that D type Flipflops were best suited for use in both circuits. These flipflop type have 4-bit inputs, so the number of flip flops needed was identified by the required states. The value 'latched' until it was reset by the input. The structure is shown below.



*NOT NECESSARY
IN THE CONCLUSION.*

The decoder was not properly tested until it was in the full test bed circuit. A clock/input could have been with the unit counter probe display in order to properly test the decoder before it entered the circuit in case problems were to arise.

One fault within the circuit is that the sequence starts on the value eleven, when ideally it should start on zero. The clock is connected to the 0-9 counter which acts as an input to the 0-5 counter. This provides a pulse from the clock which allows the tens counter to produce the value one, making the starting value eleven. If the circuit were to be used practically this would need to be fixed. It is recommended that further research would need to be conducted on components which could be added or replaced to stop this problem. A different type of design could also be created in order to get around this problem.

Overall, I think the specification was met as the counter was able to count from 0-59.

*ALWAYS USE
3RD PERSON.*

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Good List

7. Annexe for supplementary diagrams, data sheets and large results tables etc.

FINAL GRADE

GENERAL COMMENTS

Instructor

75/100

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GRADING FORM: CSG-RUBIC

TAYLOR HOSKINS

0

RESEARCH-INFORMED LITERATURE



There was very good evidence of further reading and research from credible and reliable sources. Your interpretation and understanding of the additional research was good and demonstrated a very good underlying appreciation of the subject. Your references were appropriate to the task and applied with few errors or inconsistencies. Your reference list was of an appropriate length for this assignment.

7/10

KNOWLEDGE AND UNDERSTANDING



The knowledge and understanding of the subject demonstrated by this assignment was generally very good. There were few gaps in your knowledge of the basic principles and your understanding of the higher level concepts was demonstrated to a high degree. You have demonstrated a competent critical understanding of the main concepts and expanded your knowledge beyond that contained in the course notes.

23/30

ANALYSIS



Your analysis of the task was excellent, both in class and as shown in this assignment. You have demonstrated highly competent analytical skills and your approach to the task was highly logical. You carried out a detailed evaluation of the results and included an excellent conclusion relating your practical results to accepted theory. You have demonstrated a capacity for independent thought and your interpretation of the quantitative and qualitative data was excellent with sound judgements based on wholly valid arguments.

23/30

PRACTICAL APPLICATION AND DEP.



Your application of practical skills for this task was generally excellent. You used both the basic and advanced features of the resources appropriately when designing the circuit and you used appropriate advanced options for testing and evaluating the circuit performance. You managed to design an effective circuit that functioned well within the specification and achieved this by rarely

15/20

asking for assistance thus demonstrating some advanced problem solving skills. Your results were comprehensive and allowed for a detailed conclusion to be written.

SKILLS FOR PROFESSIONAL PRAC.



In this assignment you have demonstrated skills in working individually and also collaboratively. Your written report was written in a professional and confident style, however you still need to be more efficient with your word count. The report was very well presented, with excellent diagrams in appropriate places, good sentence/paragraph structure and clear calculations.

7/10