

2017197

by Aeron Smitham

FILE	16679_AERON_SMITHAM_2017197_179157_1671346733.PDF (743.78K)		
TIME SUBMITTED	03-MAY-2021 06:24PM (UTC+0100)	WORD COUNT	4646
SUBMISSION ID	151454967	CHARACTER COUNT	22664

Course:	HNC Electrical and Electronic Engineering
Module:	SGEE4003 - Electronics1
Assignment Title:	Assignment 2 - Digital Circuit Design
Name:	Aeron Smitham
University number:	2017197
Date Submitted:	03/05/2021
Word Count:	2739 words

90+

- ① EXCELLENT RESEARCH WITH A WIDE RANGE OF APPROPRIATE SOURCES AND CORRECTLY FORMATTED CITATIONS.
- ② DESIGN METHOD WAS EXPLAINED IN DETAIL.
- ③ COMPREHENSIVE TESTING.
- ④ ANALYSIS OF RESULTS WAS EXCELLENT.
- ⑤ EXCELLENT CONCLUSIONS.

Table of Contents

1. Executive Summary.....	3
2. Introduction aims and objectives.	4
3. Research.....	5
Combinational and Sequential Logic.....	5
Finite State Machines (FSM)	7
FPGA and ASIC.....	8
4. Design method	9
7-Segment.....	9
0-5 Counter	12
0-9 Counter	14
00-59 Stopwatch	17
5. Analysis of results	18
7-Segment Display	18
0-5 Counter	19
0-9 Counter	21
00-59 Stopwatch	23
6. Conclusions	28
7. References	29
8. Annexe.	30

1. Executive Summary

This report has been an investigation into digital electronic circuits and how they are designed. The task was to build an electronic stopwatch that counts from 00-59 repeatedly, which required a combination of the two types of digital circuits: combinational and sequential logic. These two branches of digital electronics were thoroughly researched, along with Finite State Machines (FSMs), FPGAs and ASICs. The knowledge gained from the research tasks was then applied to the design of several circuits, such as the decoder circuit that used combinational logic, and the 0-5 and 0-9 counter circuits that used sequential logic and FSMs.

The software package, NI Multi-Sim was used to build and test the circuit with logic analysers used extensively to test each circuit thoroughly. All testing concluded that the circuits were functioning correctly, and the results could be seen visually as the two 7-segment displays counted from 00-59, confirming the exercise to be a success.

VERY GOOD SUMMARY.

2. Introduction aims and objectives.

This assignment introduces the subject of digital circuit design. A digital circuit is to be designed, simulated, tested, and then evaluated. Research will be conducted over several digital circuit topics, including: combinational and sequential logic; Finite State Machines (FSM); FPGAs and ASICs. The theory learnt from this research will then be applied to the design process of a digital circuit.

The objective of this assignment is to display a count of 00-59 that keeps repeating, on two 7-segment displays. Combinational logic shall be used to design a decoder, while sequential logic and a FSM will be used to design a 0-5 and 0-9 counter. These circuits will then be combined with the 7-segment displays to form a 00-59 stopwatch.

3. Research

Combinational and Sequential Logic

Digital electronics is made up of two types: combinational and sequential circuits. Combinational logic circuits are dependant entirely on the inputs of the circuit. The output state can only be realised by the combination of inputs that circuit needs. It is a memory-less circuit, which changes its state immediately once its inputs change (Storey, 2017). There are various combinational logic devices, such as: multiplexers and demultiplexers; encoders and decoders.

Multiplexers are digitally controlled switches. They usually have four pins: inputs, outputs, select and enable. In most multiplexers there are two input channels, channel A and channel B. The select pins' function is to choose which channel will be read by being either high (on) or low (off). For example, if the select pin is high then channel A's inputs will be read, and channel B's inputs will be read if the pin is low. The enable pins' function is to, however counterintuitively, disable the outputs. If the enable pin is high, then the outputs will be disabled – no matter what state the inputs are in. A truth table for a multiplexer can be seen in figure 1. Multiplexers and demultiplexers are used for simple signal mapping (element14, 2019).

TRUTH TABLE				
ENABLE	SELECT INPUT	INPUTS		OUTPUT
E	S	I ₀	I ₁	Z
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Figure 1 - (Motorola, n.d.)

For more specific applications, encoders and decoders are used to translate one form of data to another. Encoders take data at their inputs, figure out what value is being represented and output that data as binary code (Brindley, 1999). Encoders are used for positional control, detecting interrupts in microprocessors and in keyboards.

Decoders are the opposite of encoders. They take binary values and translate it to other forms of data. One use of a decoder is converting binary coded decimal into a 7-segment display, as seen in figure 2. Each segment has 1 pin and can be either high or low. When the pin is high the LED segment will light up. The segments traditionally make up a display of the numbers 0-9 but can also display the letters A-F, which can represent 10-15, as in hexadecimal (Corbeill, 2019).

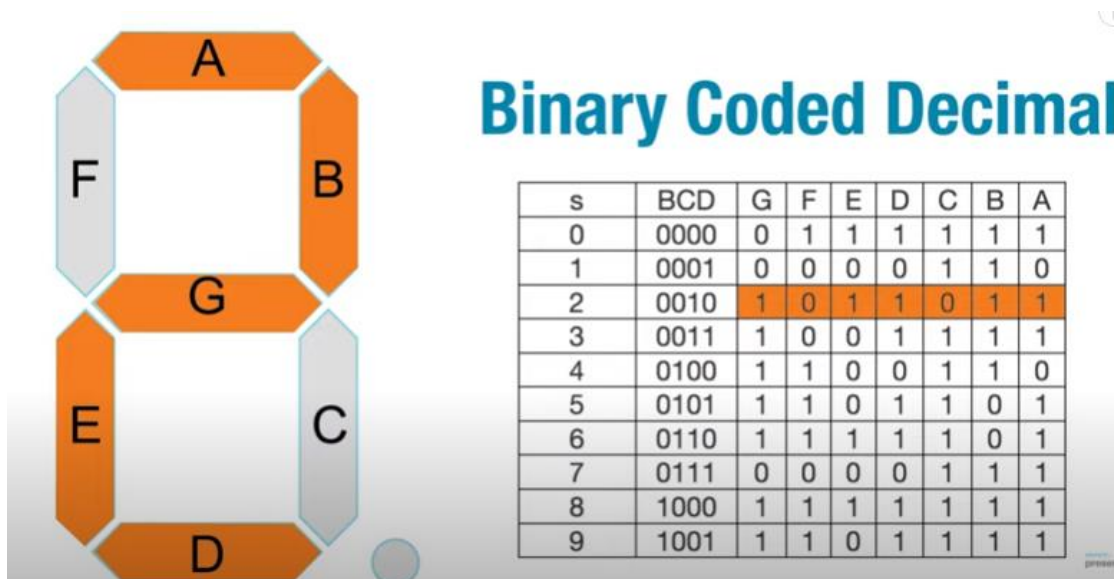


Figure 2 - (Corbeill, 2019)

Sequential logic can be seen to be similar in function to combinational logic, but with the addition of memory. Sequential logic outputs are a product of the current state of the inputs and the last state of the output, utilizing the memory aspect of sequential logic through a feedback loop (The Learning Circuit, 2019). There are various types of sequential circuits, such as: S-R latches, J-K flip-flops, and D-type flip-flops. Out of the three, the D-type is the most widely used as it is the only one that does not have any indeterminate states. Data is stored through its clock input, which stores the last output state in its memory for one cycle until the next rising edge of the clock is seen (Horowitz & Hill, 1989).

Another type of sequential circuit is an asynchronous counter. Flip-flops are cascaded, with the output of one flip-flop being the clock input of the next flip-flop. Each flip-flop represents a bit, so four flip-flops would make a 4-bit counter which can count to 15, and therefore could be used as a decade counter. Flip-flops act as a divide by two circuit, as seen in figure 3, as the output frequency is half the frequency of the input due to the time taken for 1 pulse to alter the value from 0 to 1 and vice-versa (Bishop, 2003).

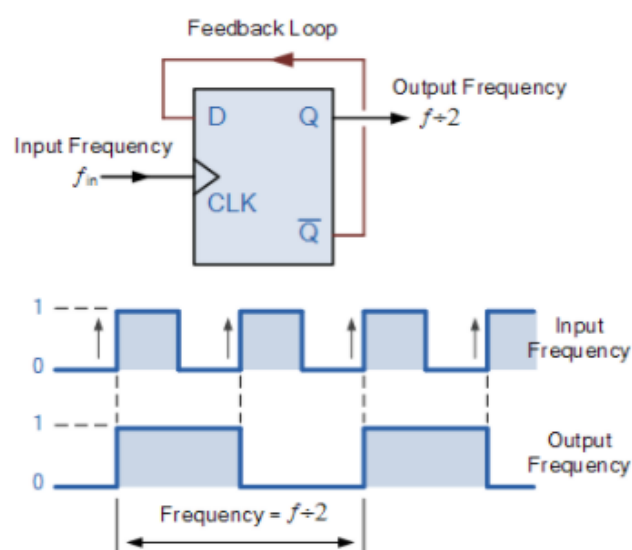


Figure 3 - (Electronics Tutorial, 2017)

Finite State Machines (FSM)

FSMs are used to design sequential logic circuits. They are not an “actual” machine but a model of how a machine will react to external events. The FSM can only be in one of a finite number of states at one time and changes when a change of input occurs. State diagrams can be drawn to visualise the FSM. Transition arrows join the states and have conditions which will cause the state to alter. State tables, which are like truth tables, can also be used and have input, output, current state and next state columns in them. Karnaugh maps are utilised to find the Boolean equation needed for the state to transition, with the equation being the basis of which the circuit is built on (Wakerly, 2019).

There are two types of FSMs: Mealy machines and Moore machines. In a Moore machine, the next state is represented inside the state bubble of a state diagram. The transition conditions are represented on the transition lines between the state bubbles, showing what is needed to progress to each state. In a Mealy machine, the next state is represented outside the state bubble with the transition condition needed for the next state to be realised. The state bubble is labelled with a number to show which state the machine is in (Jones, 1995).

A simple example of how an FSM can be used for a turnstile system can be seen in figure 4.

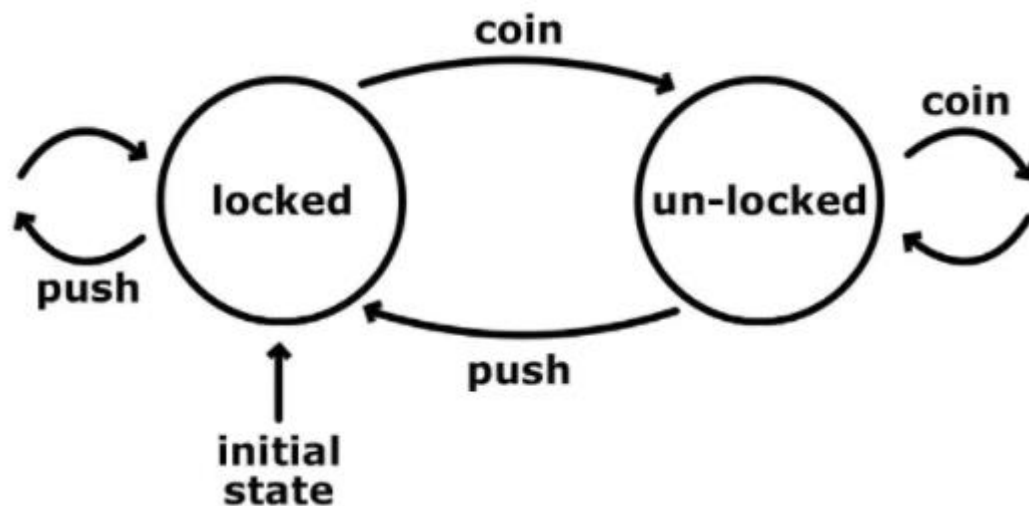


Figure 4 - (Tsonev, 2018)

FPGA and ASIC

A field programmable gate array (FPGA) is a semi-conductor integrated circuit (IC). FPGAs are programmable devices and can be reprogrammed multiple times, by a new file being downloaded and overwriting the old file. The function of a FPGA can be defined after manufacturing, meaning the device can be reconfigured even in the field, as and when it is needed. Two-dimensional arrays of logic gates are used to make up gate arrays. The reprogrammable side of FPGAs allows for their continued use, even when upgrades or modifications are needed in a system, instead of having to buy a replacement any time modifications are required (Boylestad & Nashelsky, 2014).

An application specific integrated circuit (ASIC) is a chip that is manufactured to control a specific application. Unlike a FPGA, the ASICs are not reprogrammable and once a program has been downloaded to them it cannot change. The circuit is burnt onto the chip so that no modifications can be made. As ASICs are application specific, they are cheap to buy in bulk. ASICs can include microprocessors, EEPROM, RAM and flash memory, this has led to them being described as a system-on-chip (SOC). VHDL is used to describe the functionality of an ASIC. Table 1 compares the features of both an ASIC and a FPGA.

Specifications	FPGA	ASIC
1.Time to Market	Prompt	Lengthy
2.Design	Easy	Intricate
3.Unit Cost	Expensive	Cheap
4.Performance	Mid-range	Top-range
5.Power Consumption	High	Low
6.Size	Mid-sized	Small

Table 1

EXCELLENT RESEARCH.

4. Design method

7-Segment

The specification for this task was to design a circuit that converts a binary code to a 7-segment display, with a decoder being designed to carry this out. The decoder had four inputs: A, B, C, and D, with A being the most significant bit (MSB). The four inputs represented a 4-bit binary value that could equal 0-15. The decoder had 7 outputs, with each output being a segment of the 7-segment display. A truth table (Table 2), Karnaugh maps and Boolean equations had to be used before the circuit could be built.

Decimal	Inputs				Outputs						
	A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	1	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1
X	1	0	1	0	X	X	X	X	X	X	X
X	1	0	1	1	X	X	X	X	X	X	X
X	1	1	0	0	X	X	X	X	X	X	X
X	1	1	0	1	X	X	X	X	X	X	X
X	1	1	1	0	X	X	X	X	X	X	X
X	1	1	1	1	X	X	X	X	X	X	X

Table 2

WELL PRESENTED

Segment – Karnaugh Map, Boolean Equation & Circuit	Figure
A <i>a</i>	5
B <i>b</i>	6
C <i>c</i>	7
D <i>d</i>	8
E <i>e</i>	9
F <i>f</i>	10
G <i>g</i>	11

Table 3

CAPITAL LETTERS ARE THE INPUTS.

CD \ AB	00	01	11	10
00	1	0	1	1
01	0	1	1	1
11	X	X	X	X
10	1	1	X	X

$$a = A + C + BD + \bar{B}\bar{D}$$

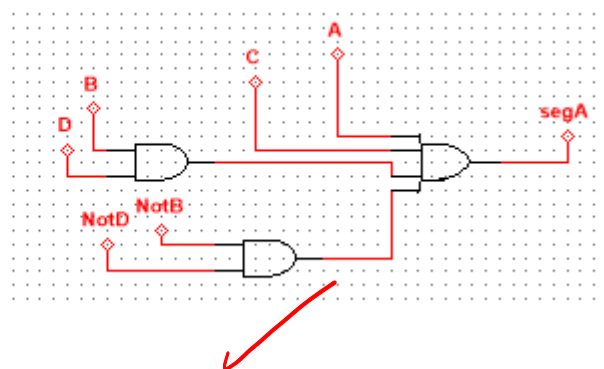


Figure 5

CD \ AB	00	01	11	10
00	1	1	1	1
01	1	0	1	0
11	X	X	X	X
10	1	1	X	X

$$b = \bar{B} + \bar{C}\bar{D} + CD$$

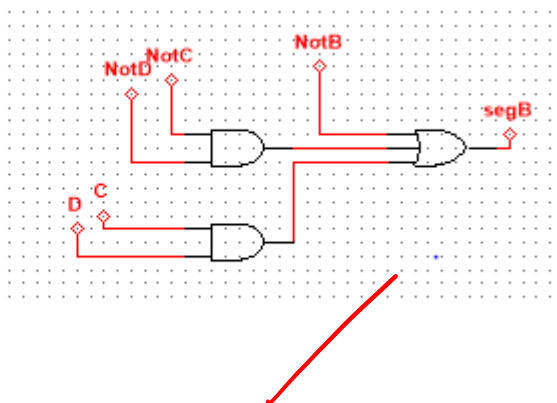


Figure 6

CD \ AB	00	01	11	10
00	1	1	1	0
01	1	1	1	1
11	X	X	X	X
10	1	1	X	X

$$c = \bar{C} + B + D$$

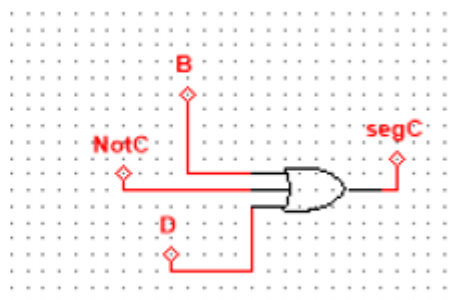


Figure 7

CD \ AB	00	01	11	10
00	1	0	1	1
01	0	1	0	1
11	X	X	X	X
10	1	1	X	X

$$d = B\bar{C}\bar{D} + \bar{B}\bar{D} + \bar{B}C + C\bar{D} + A$$

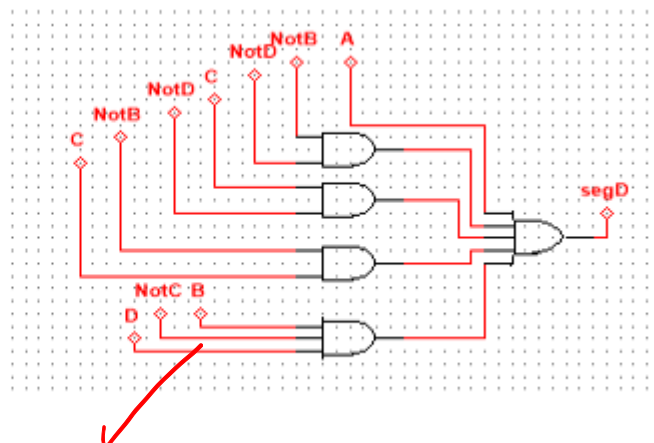


Figure 8

CD \ AB	00	01	11	10
00	1	0	0	1
01	0	0	0	1
11	X	X	X	X
10	1	0	X	X

$$e = \overline{B}\overline{D} + C\overline{D}$$

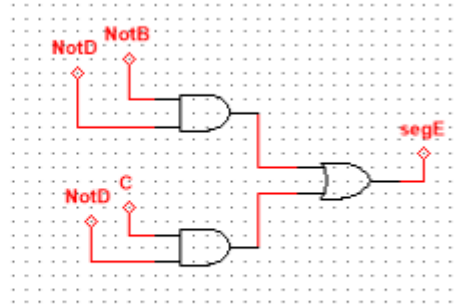


Figure 9

CD \ AB	00	01	11	10
00	1	0	0	0
01	1	1	1	1
11	X	X	X	X
10	1	1	X	X

$$f = A + B + \overline{C}\overline{D}$$

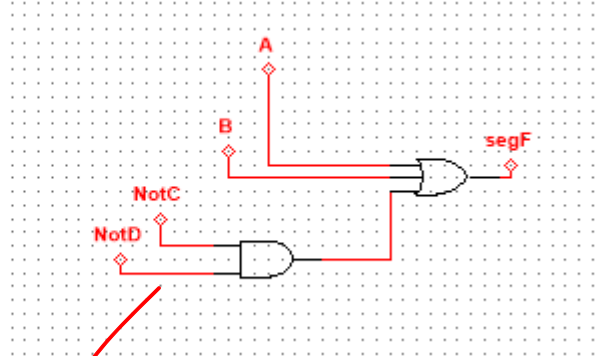


Figure 10

CD \ AB	00	01	11	10
00	0	0	1	1
01	1	1	0	1
11	X	X	X	X
10	1	1	X	X

$$g = A + C\overline{D} + \overline{B}C + B\overline{C}$$

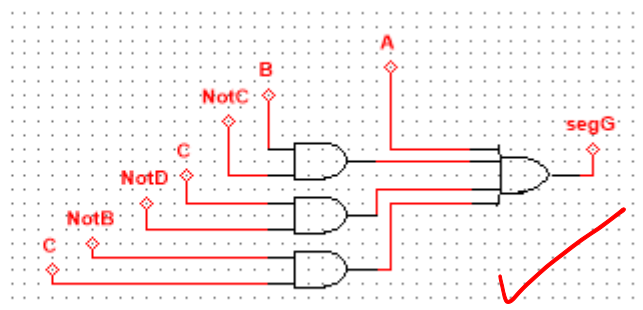


Figure 11

Figure 11 shows the Karnaugh map, Boolean equation, and circuit for segment g. The circuit is designed from the Boolean equation, and the equation is found from the Karnaugh map. The values for each row of the map are found from the table 2. All the 1's in the map must be grouped together in the largest group possible, with X's having the ability to become 1's if needed. From there whichever inputs are the same in all parts of the corresponding group get entered in the equation. For example, the blue group covers the two bottom rows of 1's and X's and the only input that remains constant is A, as it is 1 for both rows of the group. This method is used for all Karnaugh maps in this report.

✓ Good.

0-5 Counter

The specification for this task was to design a counter that repeatedly counts from 0 to 5. To complete this task a Finite State Machine was utilised to work out the sequence needed for the counter to meet the specification. The counter needed a starting point before transitioning through each state and returning to the starting point after reaching the final state. In this case, the final state was a count of 5 before returning to the starting state of count 0. The methods used to complete this were: state allocation (Table 4), state diagram and table (Table 5), Karnaugh maps and Boolean equations before building the circuit on Multi-Sim.

State Allocation	Count
State 0	0
State 1	1
State 2	2
State 3	3
State 4	4
State 5	5

Table 4

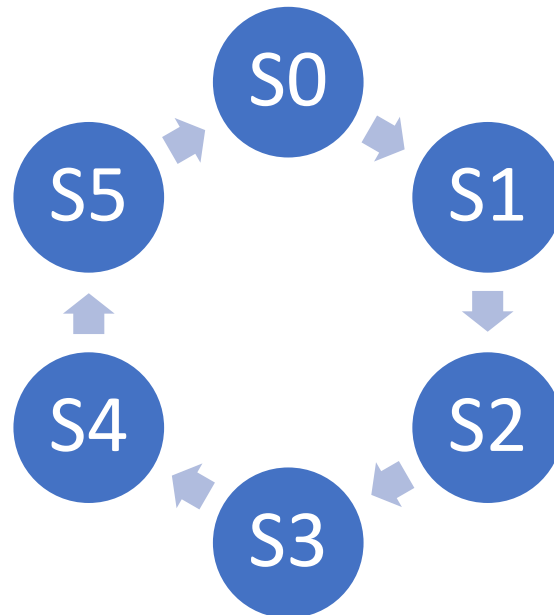


Figure 12

Current State	Next State	Current Output			Next Output		
		QA	QB	QC	QA+	QB+	QC+
S0	S1	0	0	0	0	0	1
S1	S2	0	0	1	0	1	0
S2	S3	0	1	0	0	1	1
S3	S4	0	1	1	1	0	0
S4	S5	1	0	0	1	0	1
S5	S0	1	0	1	0	0	0
S6	X	1	1	0	X	X	X
S7	X	1	1	1	X	X	X

Table 5

Output – Karnaugh Map, Boolean Equation & Circuit	Figure
QA	13
QB	14
QC	15

Table 6

QBQC \ QA	00	01	11	10
0	0	0	1	0
1	1	0	X	X

$$QA+ = QBQC + QAQC$$

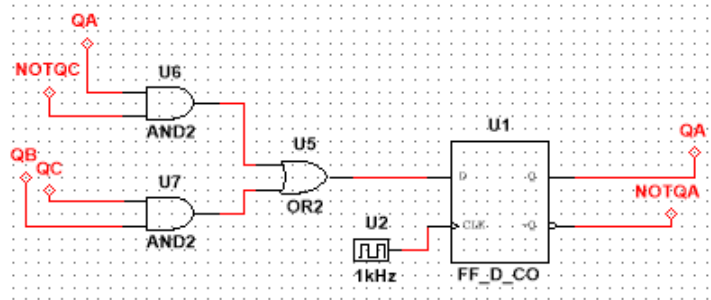


Figure 13

QBQC \ QA	00	01	11	10
0	0	1	0	1
1	0	0	X	X

$$QB+ = QBQC + QAQBQC$$

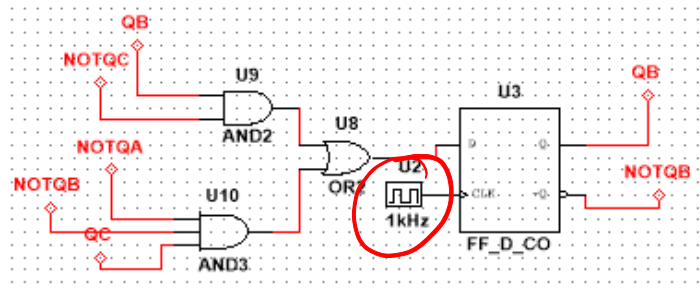


Figure 14

QBQC \ QA	00	01	11	10
0	1	0	0	1
1	1	0	X	X

$$QC+ = QC$$

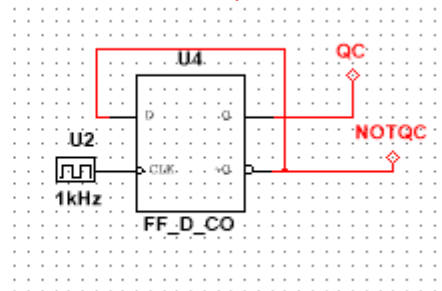


Figure 15

ONLY NEEDED IF YOU TESTED EACH CIRCUIT SEPARATELY.

0-9 Counter

The 0-9 counter was designed much in the same way as the 0-5 counter, just with the added states and output required. Zero would remain the starting state but the last state in the sequence was now 9. The additional counts needed meant an extra D-type flip-flop was needed when building the circuit. The methods used to complete this were: state allocation (Table 7), state diagram (Figure 16) and table (Table 8), Karnaugh maps and Boolean equations before building the circuit on Multi-Sim.

State Allocation	Count
State 0	0
State 1	1
State 2	2
State 3	3
State 4	4
State 5	5
State 6	6
State 7	7
State 8	8
State 9	9

Table 7

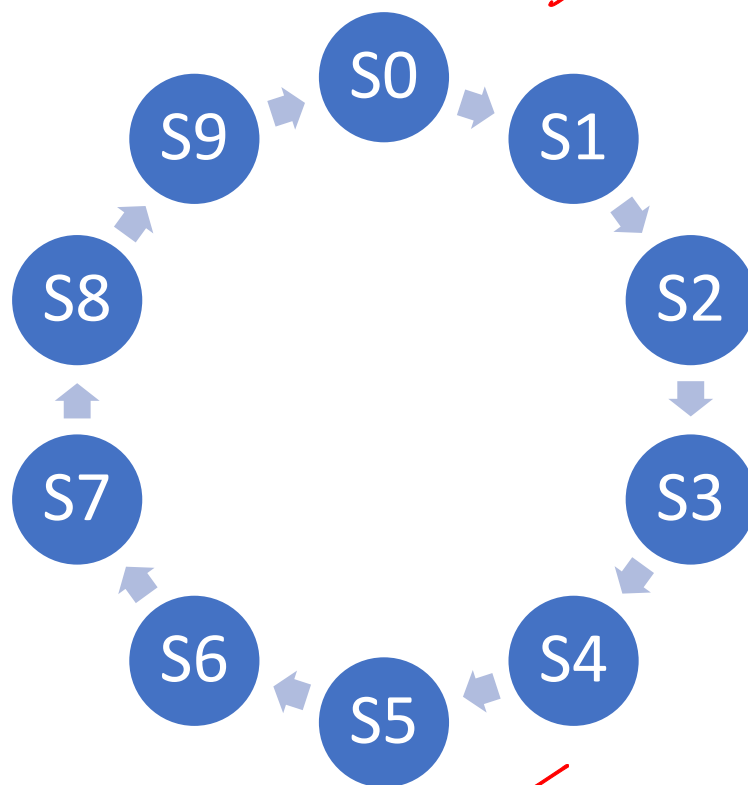


Figure 16

Current State	Next State	Current Output				Next Output			
		QA	QB	QC	QD	QA+	QB+	QC+	QD+
S0	S1	0	0	0	0	0	0	0	1
S1	S2	0	0	0	1	0	0	1	0
S2	S3	0	0	1	0	0	0	1	1
S3	S4	0	0	1	1	0	1	0	0
S4	S5	0	1	0	0	0	1	0	1
S5	S6	0	1	0	1	0	1	1	0
S6	S7	0	1	1	0	0	1	1	1
S7	S8	0	1	1	1	1	0	0	0
S8	S9	1	0	0	0	1	0	0	1
S9	S0	1	0	0	1	0	0	0	0
S10	X	X	X	X	X	X	X	X	X
S11	X	X	X	X	X	X	X	X	X
S12	X	X	X	X	X	X	X	X	X
S13	X	X	X	X	X	X	X	X	X
S14	X	X	X	X	X	X	X	X	X
S15	X	X	X	X	X	X	X	X	X

Table 8

Good.

Output – Karnaugh Map, Boolean Equation & Circuit	Figure
QA ⁺	17
QB ⁺	18
QC ⁺	19
QD ⁺	20

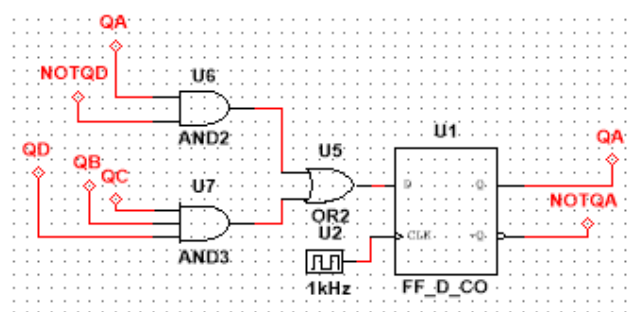
Table 9

YOU ARE FINDING NEXT STATE EQUATIONS, NOT OUTPUTS.

QCQD \ QAQB	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	X	X	X	X
10	1	0	X	X

$$QA = QA\bar{Q}\bar{D} + QB\bar{Q}CQD$$

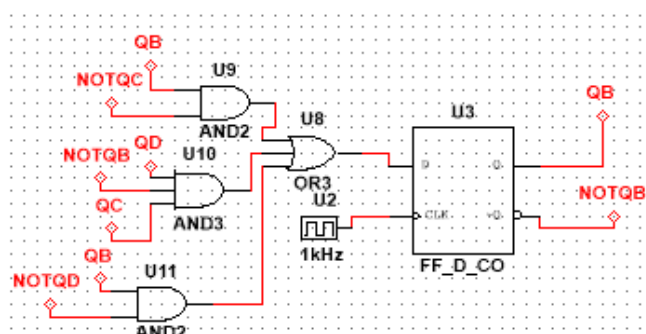
Figure 17



QCQD \ QAQB	00	01	11	10
00	0	0	1	0
01	1	1	0	1
11	X	X	X	X
10	0	0	X	X

$$QB = QB\bar{Q}C + QB\bar{Q}D + \bar{Q}BQCQD$$

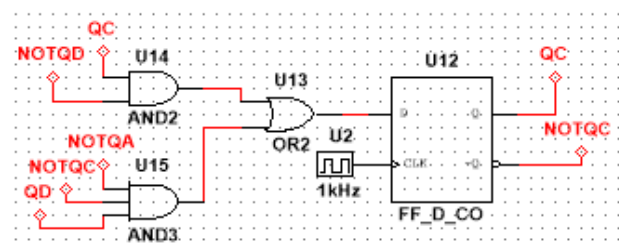
Figure 18



QCQD \ QAQB	00	01	11	10
00	0	1	0	1
01	0	1	0	1
11	X	X	X	X
10	0	0	X	X

$$QC = QC\bar{Q}D + \bar{Q}A\bar{Q}CQD$$

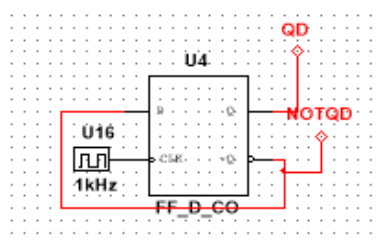
Figure 19



QCQD \ QAQB	00	01	11	10
00	1	0	0	1
01	1	0	0	1
11	X	X	X	X
10	1	0	X	X

$$QD = \bar{Q}\bar{D}$$

Figure 20



00-59 Stopwatch

The three designs were then connected in the stopwatch testbed circuit, as seen in figure 21, by inserting sub-circuits of the decoder, 0-5 counter and 0-9 counter. The decoder was used between each 7-segment display and their respective counter. The outputs from the counting sub-circuits are connected to the input of a decoder and then the outputs of the decoder are connected to their respective segments. On-page connectors are used to connect the decoder outputs to each of the 7-segment inputs, rather than directly connecting them as it makes the circuit visually clearer.

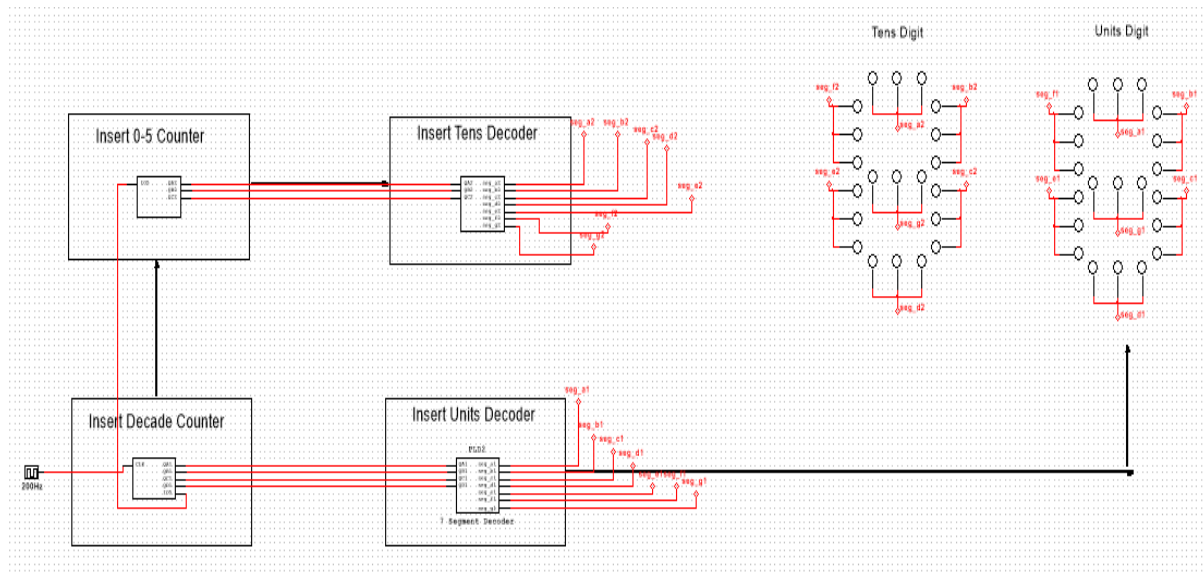


Figure 21

5. Analysis of results

7-Segment Display

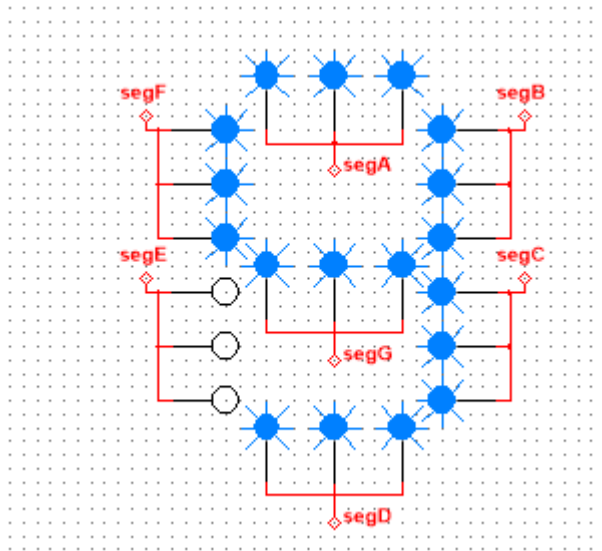


Figure 22

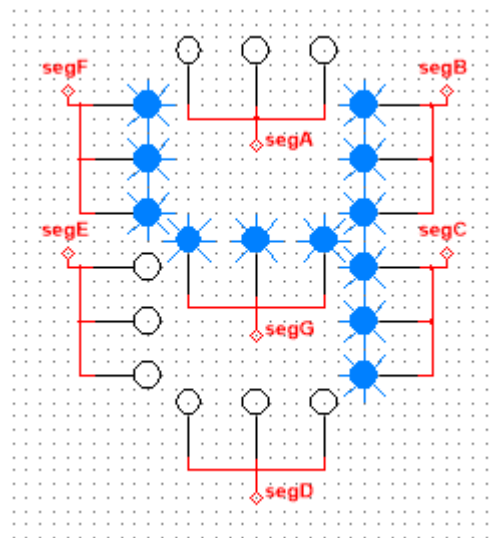


Figure 23

As seen in figures 22 and 23, the 7-segment display designed in Section 4 was completed successfully. All the segments of the display lit up and all numbers were displayed correctly. The numbers 9 and 4 are shown in figures 22 and 23, respectively. To test each segment worked the keys A, B, C and D on the keyboard were used to simulate the inputs of the same letters. By pressing each key, the input switched to on or off, altering the value being displayed on the 7-segment display. With D being the LSB of 1, and A the MSB of 8, the correct combination of keys required to increment the counter could be found. The display incremented from 0-9 by pressing the combination of keys required that equalled the relevant value.

0-5 Counter

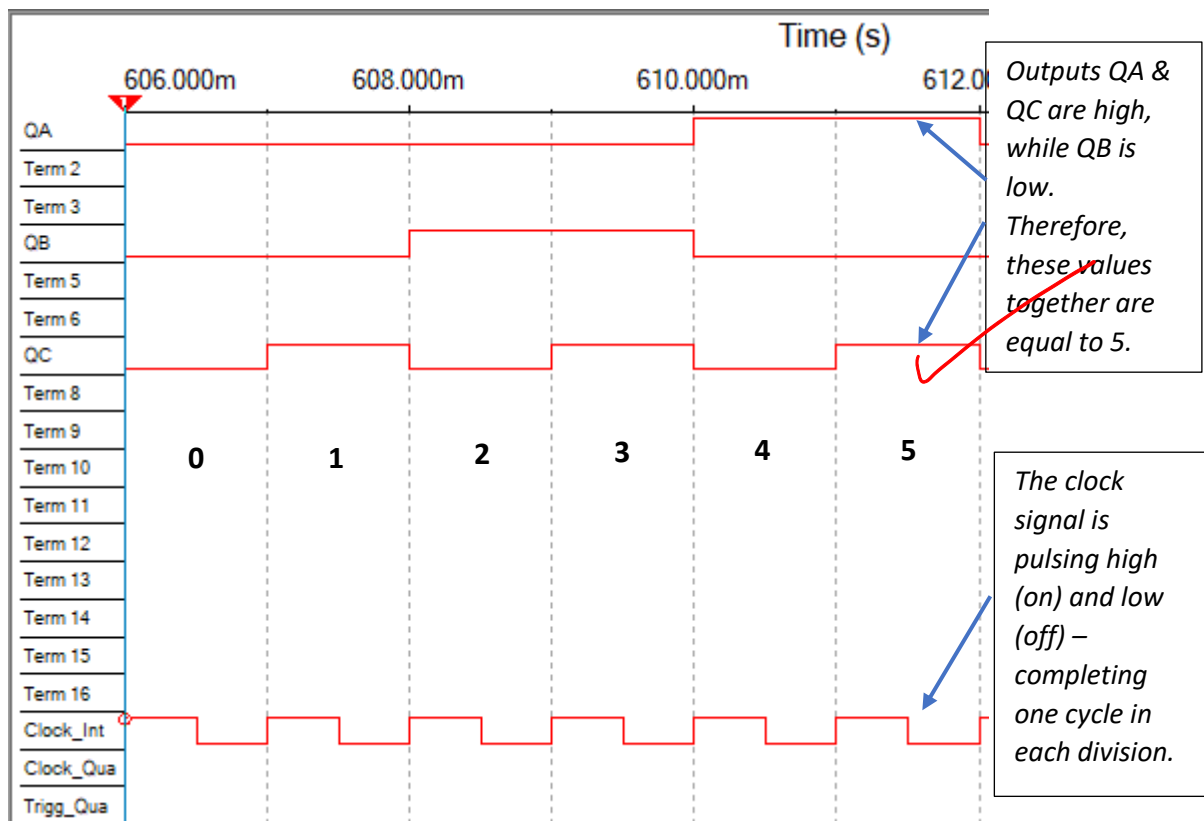


Figure 24

The logic analyser used in figure 24 shows the logic level of the outputs QA, QB and QC. The graph shows the counter incrementing one value at a time from 0-5. This has been set up by altering the clocks/div rate to show one clock cycle per division and the post trigger samples rate was changed to 20. This makes the count easier to visualise, as when the count increments it is in a separate division. The binary values of each output can be seen in table 10.

Output	Binary Value
QA	4
QB	2
QC	1

Table 10

The values are incrementing as the graph moves along the x-axis and each value has been annotated with its corresponding decimal value. Table 11 explains in detail what each value means and how it is made. Each output can either be on or off and this is displayed on the graph as the logic level being either high or low. If a combination of outputs are high, then their binary values will be added together to find out the corresponding decimal value.

Count	Outputs On	Explanation
0	None	No outputs are on, which means the binary value at that point is 0
1	QC	QC is the only output high, so as it has a binary value of 1 the decimal value is also 1
2	QB	QB is the only output high, as it has a binary value of 2 the decimal value will also be 2
3	QB & QC	QB and QC are high which means their values will be added together. Therefore, the decimal value will be 3.
4	QA	QA is the only output high, as it has a binary value of 4 the decimal value will also be 4
5	QA & QC	QA and QC are high which means their values will be added together. Therefore, the decimal value will be 5

Table 11

0-9 Counter

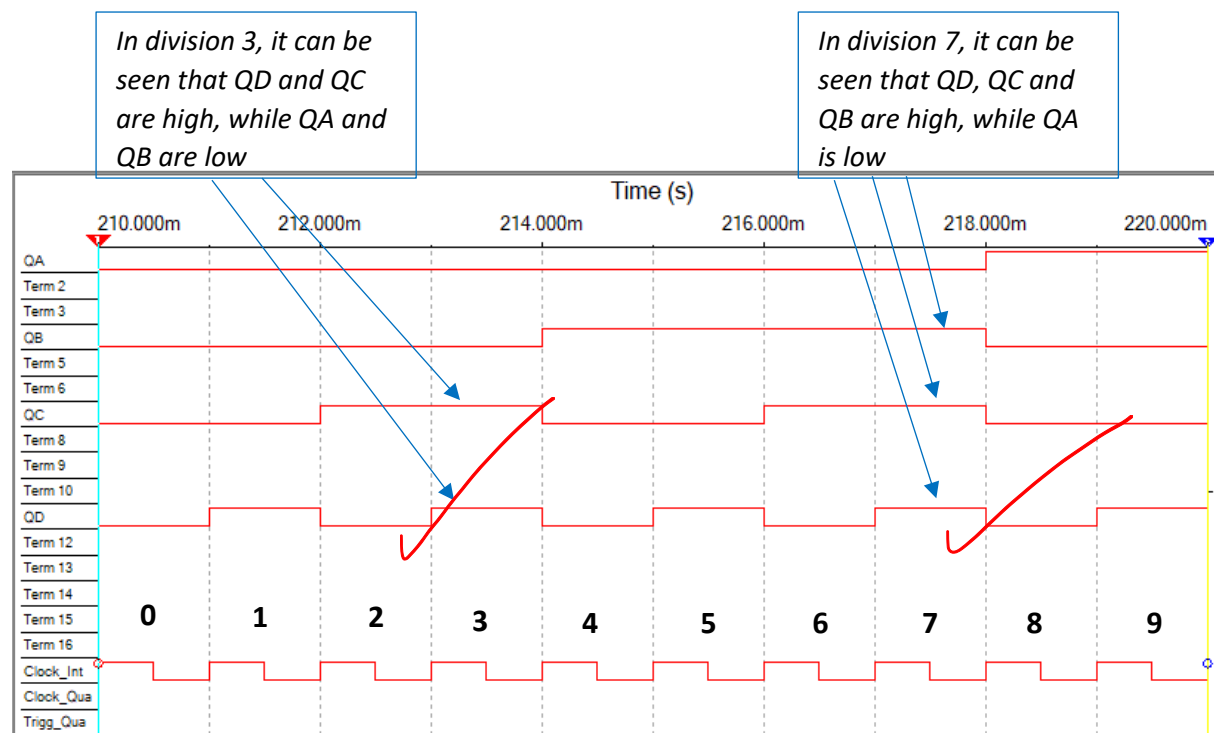


Figure 25

The logic analyser used in figure 25 shows the logic level of the outputs QA, QB, QC and QD. The clock/division rate has been set to show one clock rate per division and the post trigger samples was set to 30. This gives a clear picture of the count as each division shows the incrementing value. The readings between the two cursors show the counter incrementing one value at a time from 0-9. The binary values of each output can be seen in table 12.

Output	Binary Value
QA	8
QB	4
QC	2
QD	1

Table 12

As the graph moves along the x-axis, the count increments and each value has been annotated with its corresponding decimal value. Table 13 explains in detail what each value means and how it is made. As before, if a combination of binary values are high they will be added together to find out the corresponding decimal value.

Count	Outputs On	Explanation
0	None	No outputs are on, which means the binary value at that point is 0
1	QD	QD is the only output high, so as it has a binary value of 1 the decimal value is also 1
2	QC	QC is the only output high, as it has a binary value of 2 the decimal value will also be 2
3	QC & QD	QC and QD are high which means their values will be added together. Therefore, the decimal value will be 3.
4	QB	QB is the only output high, as it has a binary value of 4 the decimal value will also be 4
5	QB & QD	QB and QD are high which means their values will be added together. Therefore, the decimal value will be 5
6	QB & QC	QB and QC are high which means their values will be added together. Therefore, the decimal value will be 6
7	QB, QC & QD	QB, QC and QD are high which means their values will be added together. Therefore, the decimal value will be 7
8	QA	QA is the only output high, so as it has a binary value of 8 the decimal value is also 8
9	QA & QD	QA and QD are high which means their values will be added together. Therefore, the decimal value will be 9

Table 13

00-59 Stopwatch

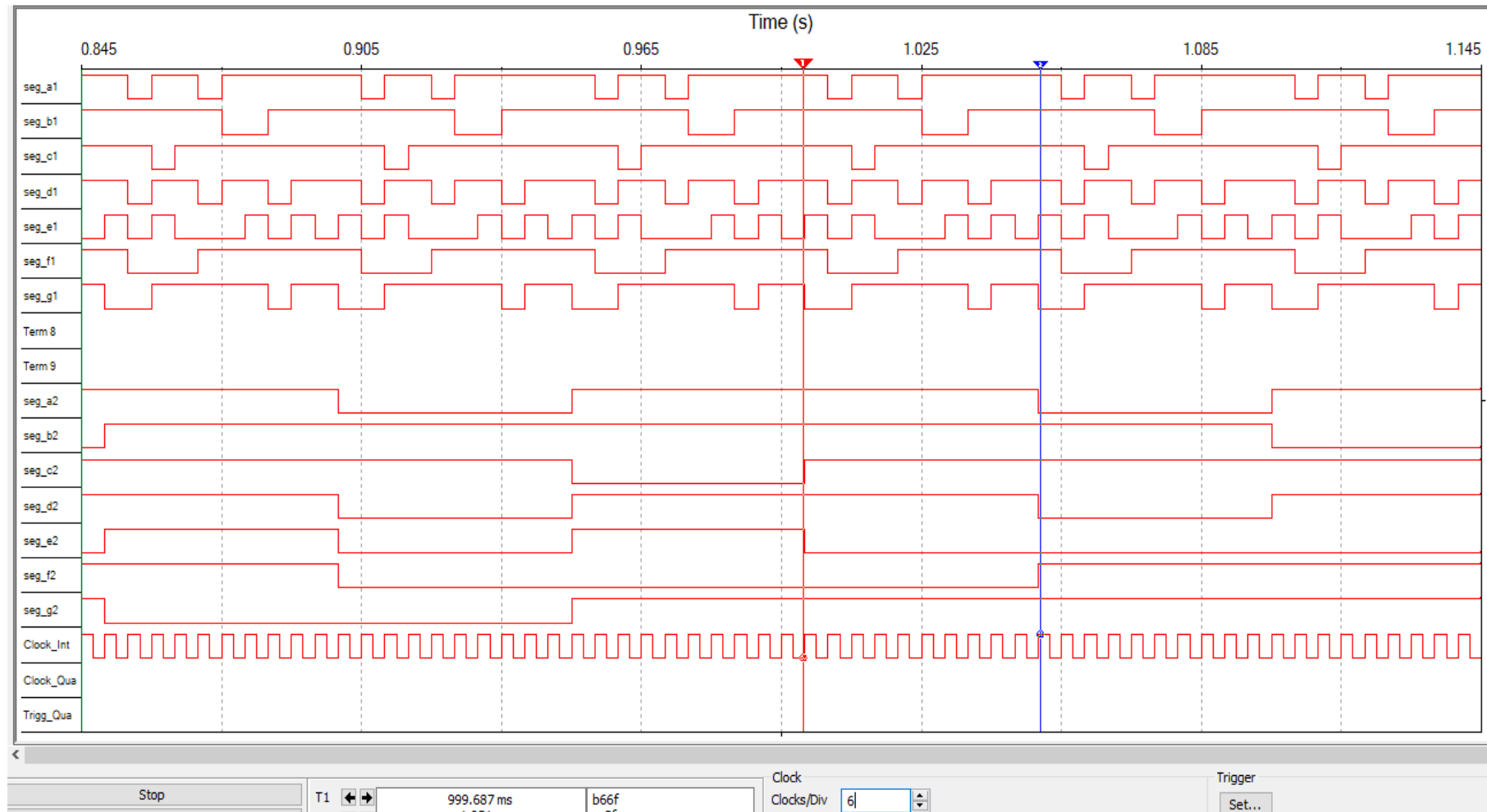


Figure 26

VERY GOOD.

Figure 26 captures the entire count, 00-59. The top 7 logic values are the units 7-segment, while the bottom 7 logic values are the tens 7-segment. The clock rate was set at 200Hz, the post trigger samples were set at 150 and the clocks per division was set to 6.

The units display can be seen to be counting 0-9 six times over for the duration of the graph cycle, while the tens display counts from 0-5 just once during the cycle. Each tens value remains the same while the units display changes from 0-9, before changing to the next tens value. Cursors have been placed on the graph between the values, 30-39. The tens display remains at 3 with the units display changing.

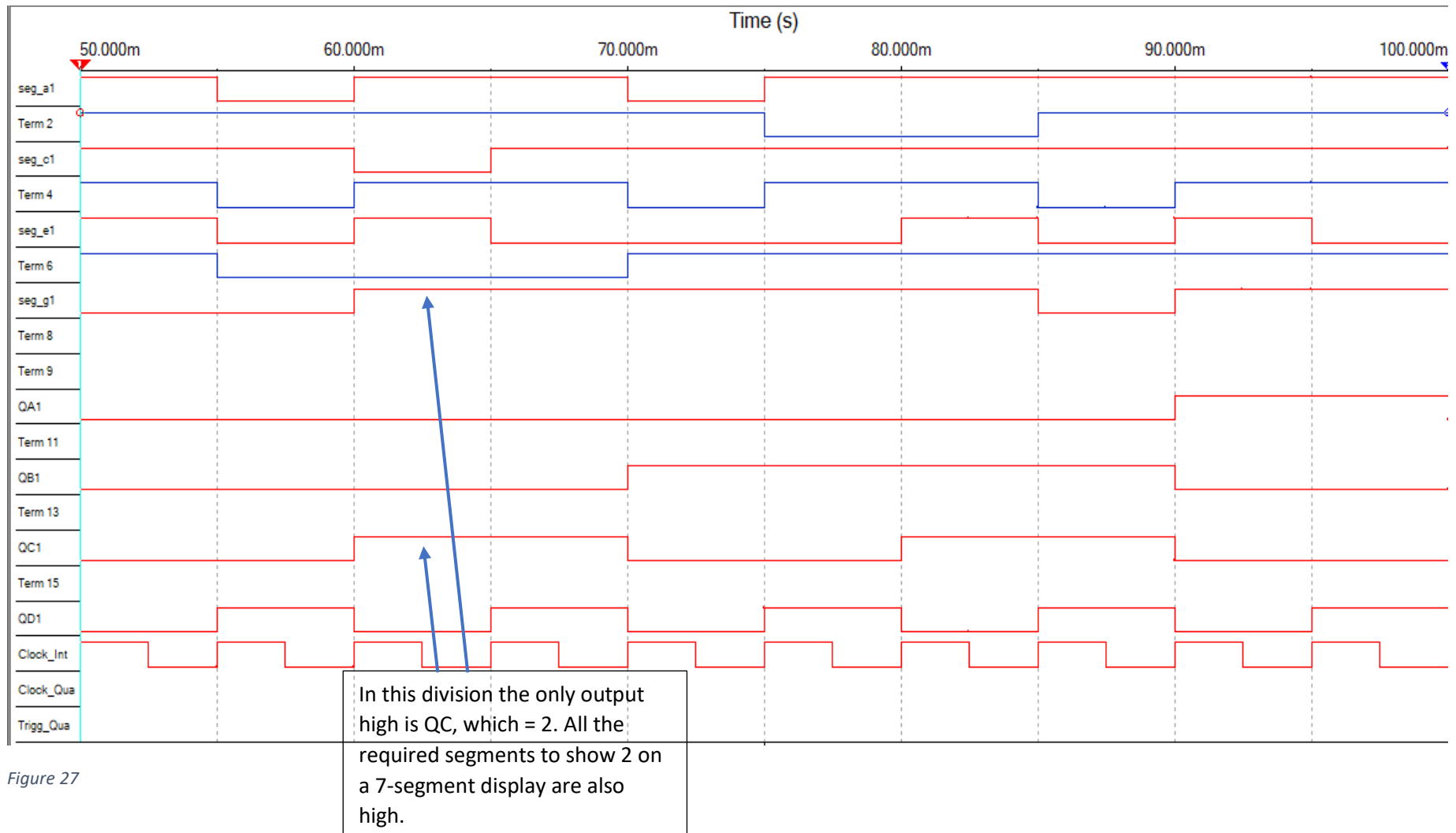


Figure 27

Figure 27 shows the 0-9 counter outputs and the 7-segment inputs on the same graph. With the clock/div set to 1, in each division from left to right are the numbers 0-9 from the counter outputs QA1, QB1, QC1 and QD1. Whatever binary value is being represented by the counter can also be seen to be represented in decimal by the top 7-segment inputs. For example, in the first division all the counter outputs are zero, therefore all but segment "seg_g1" are high which are the required segments to display the decimal number zero.

In figure 28 the same results can be seen but for the 0-5 counter and its corresponding 7-segment display.

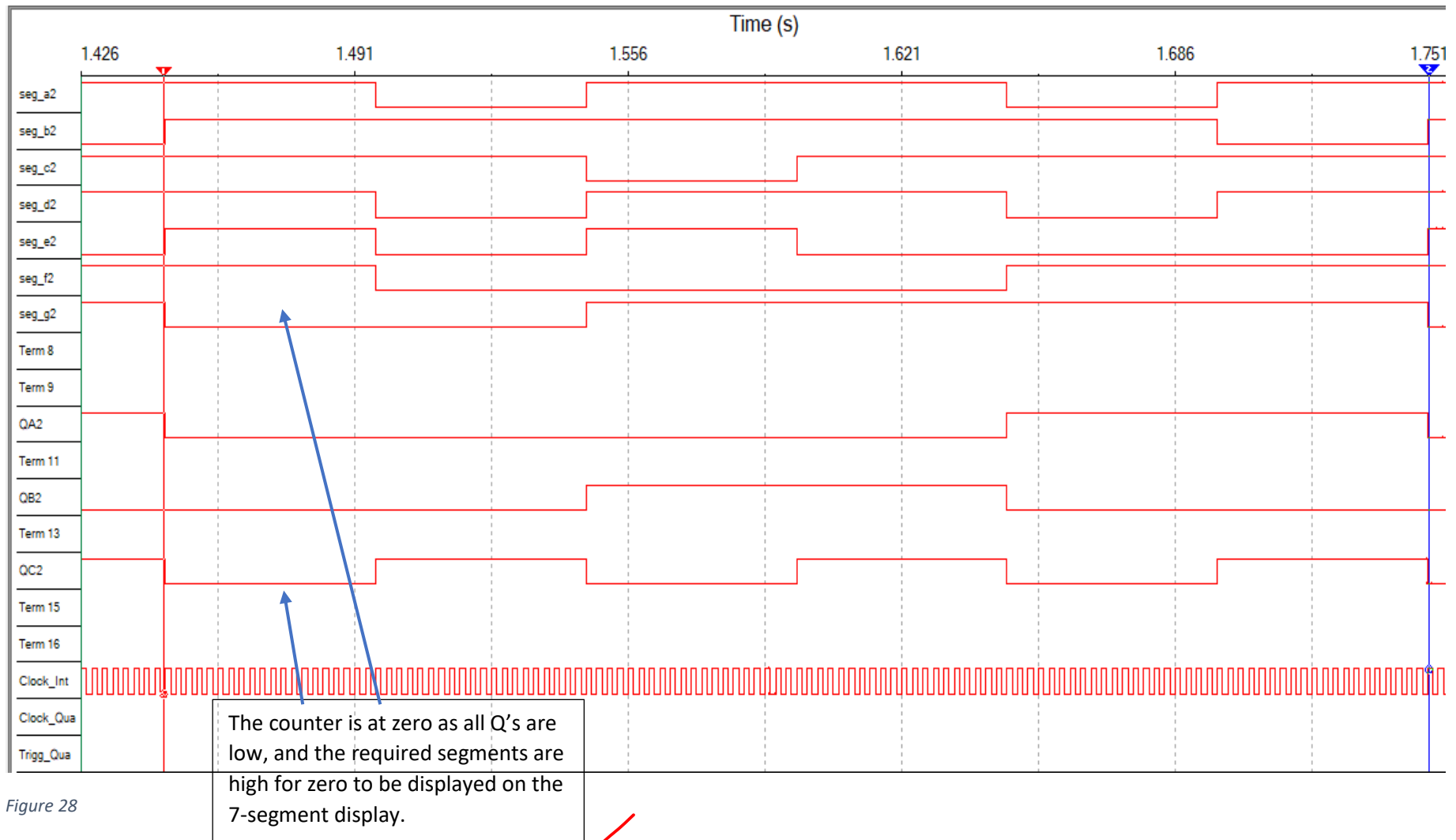


Figure 28

6. Conclusions

Combinational and sequential circuit design require different methods to be used in the design process. For sequential logic, the current state of the output must be considered before the next state can be realised. A state table is required rather than a truth table and from this the number of flip-flops or latches required can be found. For a 0-5 counter, there were six states, and three binary values were needed to represent them, and therefore three flip-flops. The three binary values – 1, 2 and 4 – allow up to eight possible states. As ten states were required for the 0-9 counter an additional flip-flop was needed, to allow up to sixteen states.

When designing combinational circuits all that must be considered is the current state of its inputs, making the design process simpler and quicker. The specification required a conversion from binary coded decimal to a 7-segment display, and as seen from the research carried out the decoder was the ideal solution for this. In the decoder circuit, one change of an input can completely alter the output – by displaying a different number on the 7-segment display.

As seen in section 5, a logic analyser was used extensively to collect results from each circuit. Any outputs that required monitoring were connected to the logic analyser, and settings such as clock rate, post-trigger samples and clocks/division were configured to display the changes of the values as the clock cycled on and off. The use of the logic analyser allowed tests to be carried out on the functioning of the circuits, displaying the outcomes on a graph so they can be manipulated to find any errors. From this, if any errors were found they could be rectified and re-tested with the analyser before progressing on to the next process in the circuit design.

An error encountered in the testing of the stopwatch was the tens 7-segment display showing the incorrect numbers. The value was starting at 20 and incrementing in 20's before displaying random segments on the display. The 0-5 counter supplying was retested – as it was previously working – and it was still counting correctly. All the connections between the counter and decoder, and between the decoder and 7-segment display were correct. Upon further investigation, it was found the inputs were valued wrong at the decoder – the most significant bit (MSB) “A” was being used instead of the least significant bit (LSB) “D”. The binary values being used were therefore: A=8, B=4 and C=2. Instead of the required: B=4, C=2 and D=1. Once this problem was solved the stopwatch began working correctly.

An improvement that this assignment could benefit from is the addition of a practical task that utilises an EEPROM for the combinational logic that is needed and compare the design method with the Multi-Sim method. The EEPROM could be pre-programmed to suit the circuit needed and its outputs could be connected straight to the 7-segment display. The results of both the simulated task and the practical task could then be evaluated to determine any different results, how the design process differs, and which method is the most suitable.

EXCELLENT WORK.

7. References

Bird, J., 2017. *Electrical and Electronic Principles and Technology*. 6th ed. Abingdon: Routledge.

Bishop, O., 2003. *Electronics: A First Course*. 1st ed. Oxford: Newnes.

Boylestad, R. & Nashelsky, L., 2014. *Electronic Devices and Circuit Theory*. 11th ed. Harlow: Pearson.

Brindley, K., 1999. *Starting Electronics*. 2nd ed. Oxford: Newnes.

Corbeill, K., 2019. *The Learning Circuit*. [Online]

Available at: <https://www.element14.com/community/docs/DOC-93330/l/the-learning-circuit-53-how-to-drive-a-7-segment-display>

[Accessed 02 04 2021].

Electronics Tutorial, 2017. *The D-Type Flip-Flop*. [Online]

Available at: https://www.electronics-tutorials.ws/sequential/seq_4.html

[Accessed 15 04 2021].

element14, 2019. *element14*. [Online]

Available at: <https://www.element14.com/community/docs/DOC-93248/l/the-learning-circuit-52-combinational-logic-devices>

[Accessed 25 03 2021].

Horowitz, P. & Hill, W., 1989. *The Art Of Electronics*. 2nd ed. Cambridge: Cambridge University Press.

Jones, M. H., 1995. *A Practical Introduction to Electronic Circuits*. 3rd ed. Cambridge: Cambridge University Press.

Motorola, n.d. *Elektronik Lager*. [Online]

Available at: <https://www.uni-kl.de/elektronik-lager/417724>

[Accessed 06 04 2021].

Storey, N., 2017. *Electronics: A Systems Approach*. 6th ed. Harlow: Pearson Education.

The Learning Circuit, 2019. *The Learning Circuit*. [Online]

Available at: <https://www.element14.com/community/docs/DOC-93709/l/the-learning-circuit-60-how-flip-flops-work>

[Accessed 07 04 2021].

Tsonev, K., 2018. *The Rise of the State Machine*. [Online]

Available at: <https://www.smashingmagazine.com/2018/01/rise-state-machines/>

[Accessed 09 04 2021].

Wakerly, J. F., 2019. *Digital design: Principles and Practices*. 5th ed. London: Pearson.

A VERY WIDE RANGE
OF SOURCES.

8. Annexe.

FINAL GRADE

GENERAL COMMENTS

Instructor

94/100

PAGE 1

PAGE 2

PAGE 3

PAGE 4

PAGE 5

PAGE 6

PAGE 7

PAGE 8

PAGE 9

PAGE 10

PAGE 11

PAGE 12

PAGE 13

PAGE 14

PAGE 15

PAGE 16

PAGE 17

PAGE 18

PAGE 19

PAGE 20

PAGE 21

PAGE 22

PAGE 23

PAGE 24

PAGE 25

PAGE 26

PAGE 27

PAGE 28

PAGE 29

PAGE 30

GRADING FORM: CSG-RUBIC

AERON SMITHAM

0

RESEARCH-INFORMED LITERATURE



There was evidence of considerable further reading and research from highly credible and reliable sources. Your interpretation and understanding of the additional research was exceptional and demonstrated a deep underlying appreciation of the subject. Your references were consistently applied to a high level of competency and your reference list was extensive for this assignment.

10/10

KNOWLEDGE AND UNDERSTANDING



The knowledge and understanding of the subject demonstrated by this assignment was exceptional. There were no gaps in your knowledge of the basic principles and the higher level concepts were extremely well explained. Your explanation of the design process and calculations was also excellent and you have demonstrated an exceptionally detailed knowledge and critical understanding of the main concepts and expanded your knowledge beyond that contained in the course notes.

28/30

ANALYSIS



Your analysis of the task was outstanding, you have demonstrated highly competent analytical skills and your approach to the task was highly logical. You carried out a detailed evaluation of the results and included an excellent conclusion connecting ideas and providing logical and persuasive arguments. You have demonstrated a considerable capacity for independent thought and the ability to see beyond the question and your interpretation of the quantitative and qualitative data was exceptional with sound judgements based on wholly valid arguments.

27/30

PRACTICAL APPLICATION AND DEP.



Your application of practical skills for this task was generally exceptional. You used both the basic and

19/20

advanced features of the resources appropriately when designing the circuit and you used appropriate advanced options for testing and evaluating the circuit performance. You managed to design an effective circuit that functioned well within the specification and achieved this by rarely asking for assistance thus demonstrating some advanced problem solving skills. Your results were comprehensive and allowed for a detailed conclusion to be attempted.

SKILLS FOR PROFESSIONAL PRAC.



In this assignment you have demonstrated skills in working individually and also collaboratively. Your written report was exceptionally well structured and written in a highly coherent and logical way. The report was presented in a professional manner using appropriate language and formatting, good diagrams in appropriate places, good sentence/paragraph structure and clear calculations.

10/10