

2017196

by Jack Rogers

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Course: HNC Electrical and Electronic Engineering
Module: SGEE4003 – Electronics I
Assignment: Assignment 2 – Digital Circuit Design
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45-50

- ① RESEARCH WAS GOOD, BUT CITATIONS WERE NOT IN THE CORRECT FORMAT. RANGE OF SOURCES COULD BE WIDER.
- ② DESIGN METHOD WAS NOT IN A LOGICAL ORDER. YOU ALSO NEEDED TO SHOW THE K-MAP GROUPS AND EXPLAIN HOW THE BOOLEAN EQUATIONS ARE DEDUCED.
- ③ SOME BASIC TESTING WAS INCLUDED IN THE ANSWER, BUT YOU HAVEN'T USED THE LOGIC ANALYSER.
- ④ WITH NO LOGIC ANALYSER GRAPHS, ANALYSIS OF RESULTS IS LIMITED.
- ⑤ SOME REASONABLE CONCLUSIONS CONSIDERING THE LACK OF TESTING.

Table of Contents

Table of Contents.....	2
Table of Figures.....	3
Introduction, Aims and Objectives	4
Research.....	5
Part A.....	5
Combinational Logic.....	5
Sequential Logic	5
Part B.....	5
Part C.....	6
FPGA's	6
ASIC's.....	6
Design Method.....	7
Truth Table.....	7
Karnaugh Maps	8
Decade Counter	9
Units Decoder	10
0-5 Counter	11
Tens Decoder	12
Digital Stopwatch Testbed	13
Analysis of Results.....	14
Conclusion.....	15
Bibliography	16
Annexe for Supplementary Diagrams, Data Sheets and Large Results Tables etc.	17

Table of Figures

Figure 1 - Combinational Logic	5
Figure 2 - Sequential Logic	5
Figure 3 - FPGA's	6
Figure 4 - ASIC's	6
Figure 5 - 7 Segment Display	7
Figure 6 - Decade Counter	9
Figure 7 - Units Decoder	10
Figure 8 - (0-5) Counter	11
Figure 9 - Tens Decoder	12
Figure 10 - Digital Stopwatch	13
Figure 11 - Simulation Test 1	17
Figure 12 - Simulation Test 2	17
Figure 13 - Simulation Test 4	18
Figure 14 - Simulation Test 3	18
Figure 15 - Simulation Test 5	19
Figure 16 - Simulation Test 6	19

Introduction, Aims and Objectives

This report will include a various of different research tasks such as two different types of logic circuits, the different types of IC chips which are known as FPGA's and ASIC's, decoders + encoders and how they are combined into a circuit. Also, in this report there will be a completion of Karnaugh maps and truth tables. Also, there will be evidence to show that a digital stopwatch was designed and simulated on a software called multisim. At the near end of the report, there will be an analysis of results and also a conclusion.

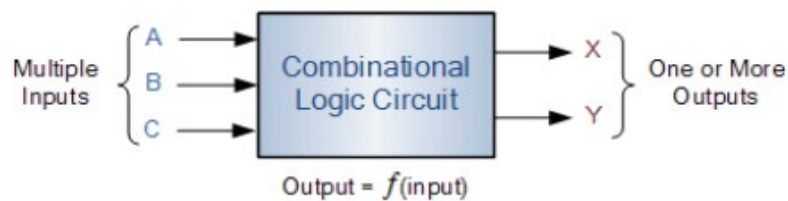
AIMS - WHAT YOU WILL DO
OBJECTIVES - HOW YOU WILL DO IT.

Research

Part A

Combinational Logic

This is made up with several different gates such as NAND, NOT or NOR that are then connected (combined) together in order to create more advanced switching circuits. These gates then get used to create an output and the previous state has no influence on the output, this is because when the inputs are sent in the circuit there is no feedback. The outputs are usually determined by a logical function of their current state, this means that it can either be a logic 0 or 1.



(Tutorials, 2021)

Sequential Logic

This type of circuit will include a memory and also give a feedback, this will then have an influence and effect the output. Although this circuit contains a combinational circuit inside it also has an extra input that goes through a flipflop. This is then used as the memory and why it will be useful for creating a digital stopwatch. In order for this circuit to work it will require a clock signal so that it can function.

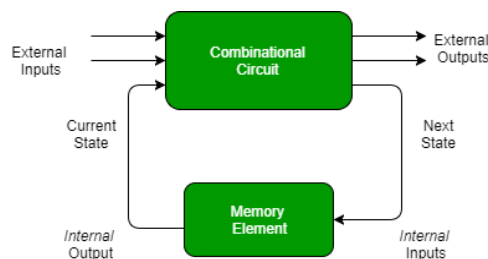


Figure 2 - Sequential Logic

(Tutorials, Electronic Tutorials, 2021)

Part B

A finite state machine is implemented with software and hardware which is used to simulate sequential logics and other programs for computing. This also has a use for understanding the decision making and the use of logic in order to control digital systems. It can also be used to solve and calculate problems. Also, with this particular method the outputs and the next state of the system is shown. This method shows you the outputs and the next state of the system. There are many different types of applications for this system such as every day uses like designing traffic lights systems, vending machines.

(Karleigh Moore, 2021)

Part C

FPGA's

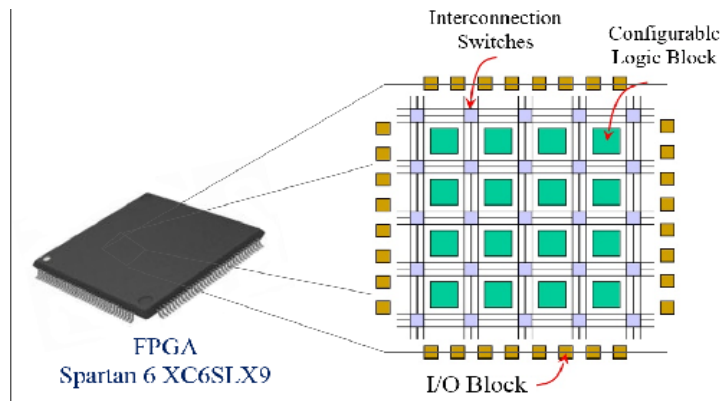


Figure 3 - FPGA's

FPGA is a chip that is a semiconductor and then can be programmed after it has been made by the manufacturer. These chips also contain many switch blocks, I/O pads, interconnector switches and logic blocks.

Advantages

- One benefit is that it can be programmed. This is good because it means that a quickly assembled circuit can be built as it can be put into a product easily and when it comes to fault finding and there is one with the chip then it can be replaced. This is not the same case as a nonprogrammable chip.
- Another good factor is that these types of chips can be reprogrammed, therefore if a fault was to occur within the chip then it can have a software change.
- Also its output pads can be used as input pads as it can solve many routing problems, this is because there will be no problem of getting all of the connections and having to use links.

(World, 2012)

ASIC's



Figure 4 - ASIC's

This chip is a non-standard integrated circuit, this means that is usually designed for special uses or specific applications. ASIC's are designed for a product that will contain a big run of production, this is because the amount of chips that are needed counter act with the high volume of production. This may also contain most of the electronics that would be needed on a single chip. One downside to using this type of circuit is that it comes at a very high cost as it is such an advanced chip. When it comes to mass manufacture it is good because the pin layout is correct for the product. These types of chips can't be modified, they also include analogue and digital control.

(Notes, 2021)

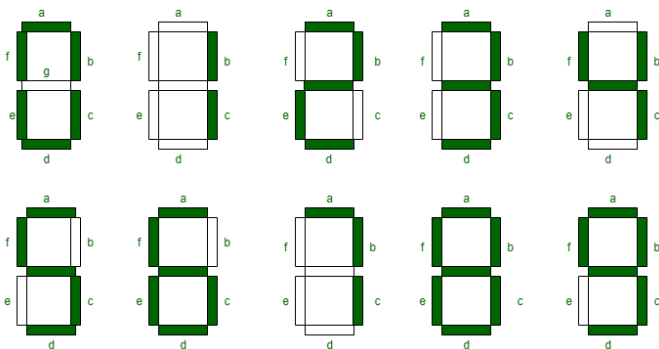
GOOD RESEARCH.

Design Method

Truth Table

Before the circuit was designed the first step was to create a truth table as this is usually the best way to help make the circuit and understand it as it will also help create Karnaugh maps. As shown below it is clear to see that this is the truth table that was constructed for the encoder of the circuit.

Decimal	Binary Inputs				Outputs						
	<i>A</i>	<i>B</i>	<i>C</i>	<i>D</i>	<i>a</i>	<i>b</i>	<i>c</i>	<i>d</i>	<i>e</i>	<i>f</i>	<i>g</i>
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	0
7	0	1	1	1	1	1	1	0	0	1	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1
N/A	1	0	1	0	X	X	X	X	X	X	X
N/A	1	0	1	1	X	X	X	X	X	X	X
N/A	1	1	0	0	X	X	X	X	X	X	X
N/A	1	1	0	1	X	X	X	X	X	X	X
N/A	1	1	1	0	X	X	X	X	X	X	X
N/A	1	1	1	1	X	X	X	X	X	X	X



After creating the truth table above it can then be used to make the Karnaugh maps. The results from the Karnaugh maps will then be used so that the creation of the encoder circuit can be done. As shown on the left here is an image of the configuration of which letters go where and what ones come on for each number. Having an image such as this one can be helpful as it can help with fault finding. For example, if the number 8 wasn't correct and a part of it wouldn't light up then you can find out which letter it is and check the circuit for that letter.

Figure 5 - 7 Segment Display

Karnaugh Maps

After looking at the truth table that was made, then the Karnaugh maps had to be constructed as seen below.

A	00	01	11	10
00	1	0	1	1
01	0	1	1	1
11	* ✗	* ✗	* ✗	* ✗
10	1	1	* ✗	* ✗
B	00	01	11	10
00	1	1	1	1
01	1	0	1	0
11	1	0	1	0
10	1	0	1	1
C	00	01	11	10
00	1	1	1	0
01	1	1	1	1
11	*	*	*	*
10	1	1	*	*

? no X's

D	00	01	11	10
00	1	0	1	1
01	0	1	0	1
11	*	*	*	*
10	1	1	*	*

E	00	01	11	10
00	1	0	0	1
01	0	0	0	1
11	*	*	*	*
10	1	0	*	*
F	00	01	11	10

00	1	0	0	0
01	1	1	1	1
11	*	*	*	*
10	1	1	*	*
G	00	01	11	10
00	0	0	1	1
01	1	1	0	1
11	*	*	*	*
10	1	1	*	*

YOU NEEDED TO SHOW
THE GROUPING AND
THE BOOLEAN EQUATIONS
ARE DEDUCED.

Decade Counter

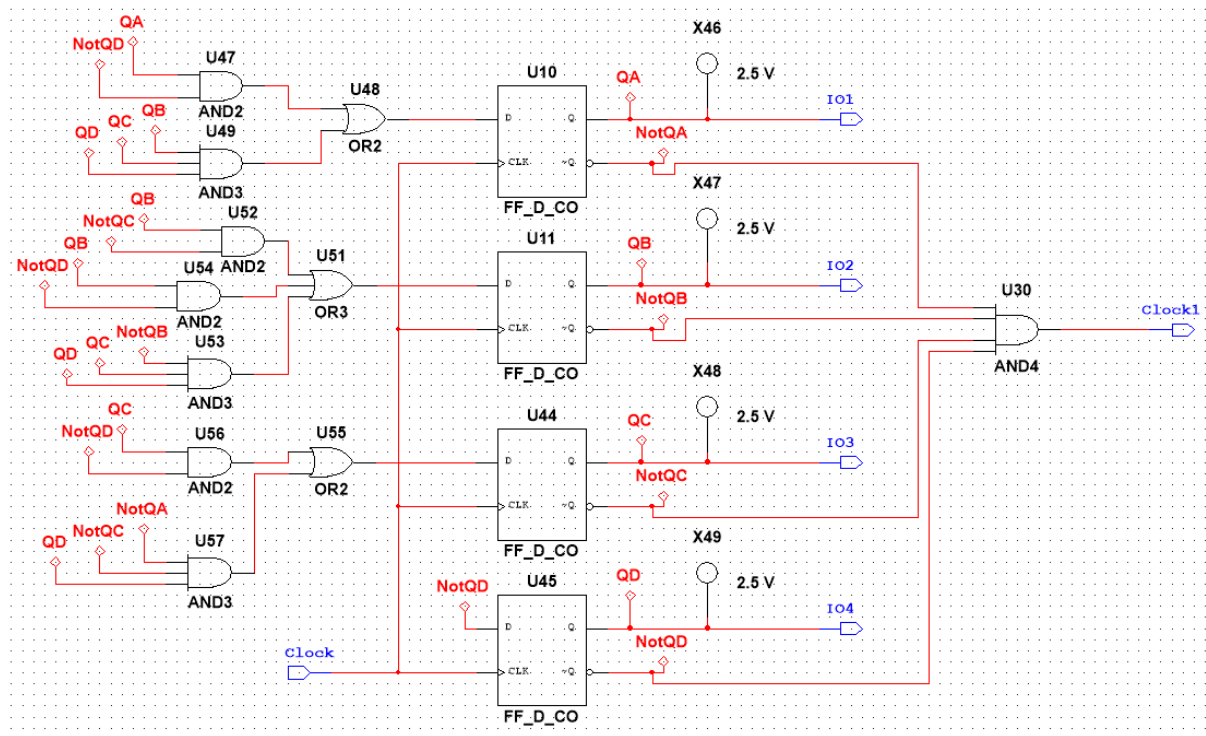


Figure 6 - Decade Counter

As shown above, its clear to see that the decade counter was constructed. In this circuit there are 1 input and 5 output connectors. This circuit is made up of AND + OR gates and clocks. This circuit will do the count from 0-9 in the stopwatch as it is called the decade counter. This circuit was also constructed by the Karnaugh maps shown below.

QA	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	*	*	*	*
10	1	0	*	*
QB	00	01	11	10
00	0	0	1	0
01	1	1	0	1
11	*	*	*	*
10	0	0	*	*

QC	00	01	11	10
00	0	1	0	1
01	0	1	0	1
11	*	*	*	*
10	0	0	*	*
QD	00	01	11	10
00	1	0	0	1
01	1	0	0	1
11	*	*	*	*
10	1	0	*	*

GROUPING AND EQUATIONS
MISSING.

Units Decoder

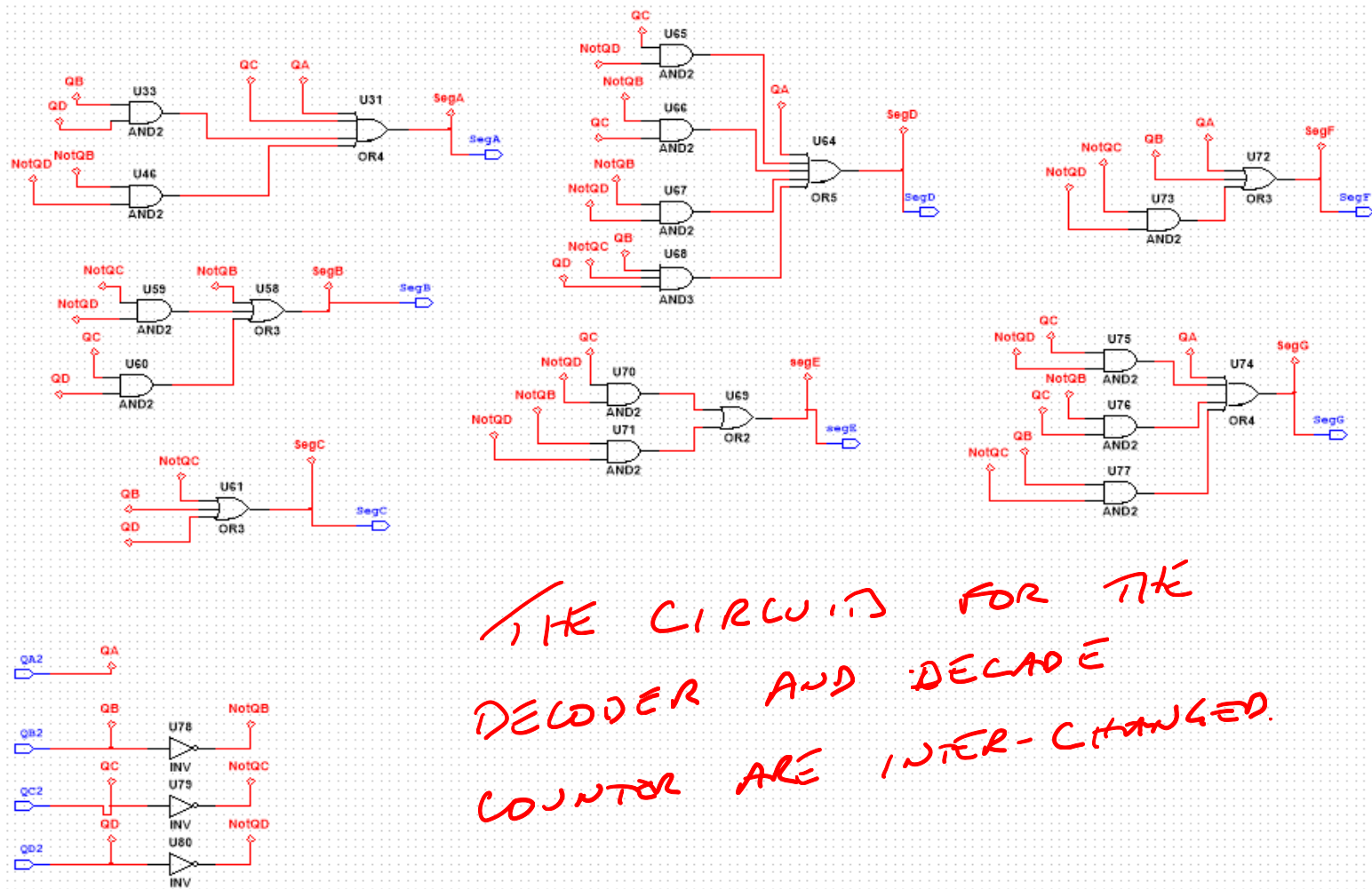


Figure 7 - Units Decoder

As shown above, this is units decoder. This circuit is used to display the 7 different segments on the 0-9 counter on the stopwatch.

0-5 Counter

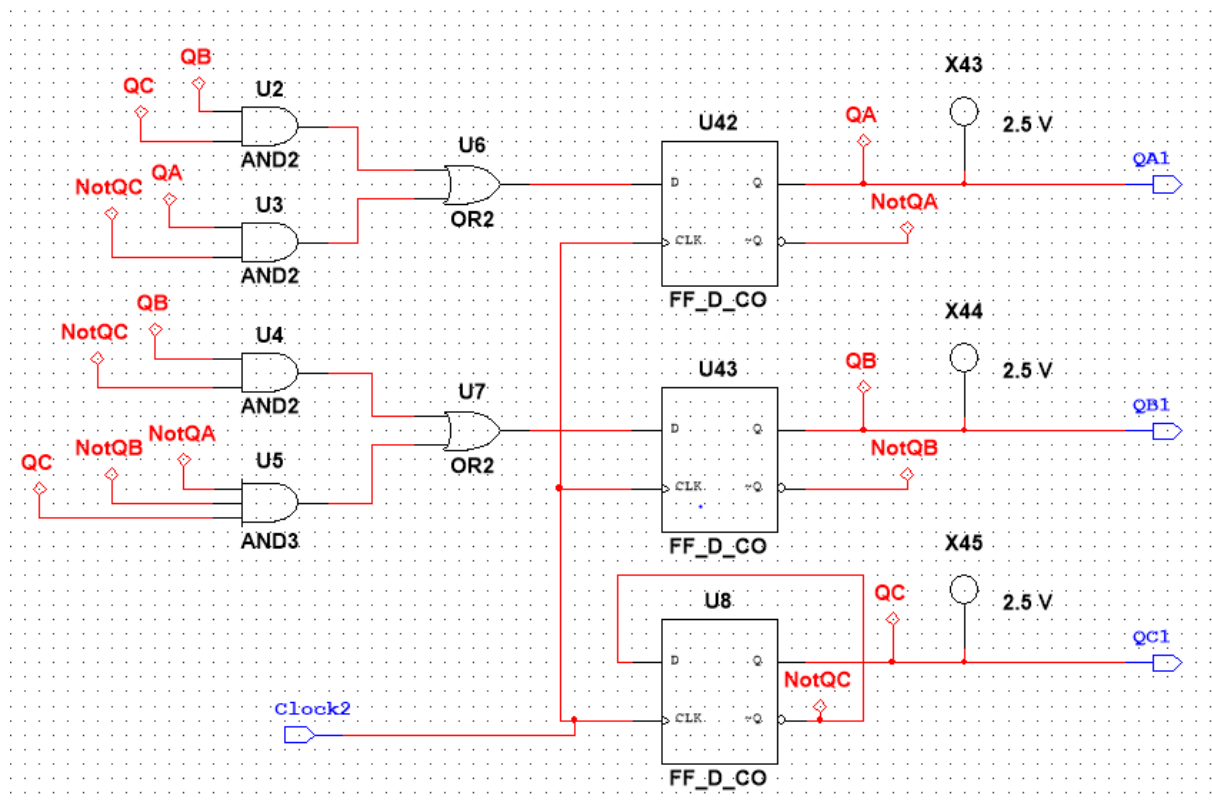


Figure 8 - (0-5) Counter

This circuit is used for the 0-5 counter for the stopwatch. By looking at the image above you can see that there are 1 Input and 3 Output connectors in the subscribed circuit. Also, this circuit was designed by using the Karnaugh Maps below.

QA	00	01	11	10
0	0	0	1	0
1	1	0	X	X
QB	00	01	11	10
0	0	1	0	1
1	0	0	X	X

Qc	00	01	11	10
0	1	0	0	1
1	1	0	X	X

Tens Decoder

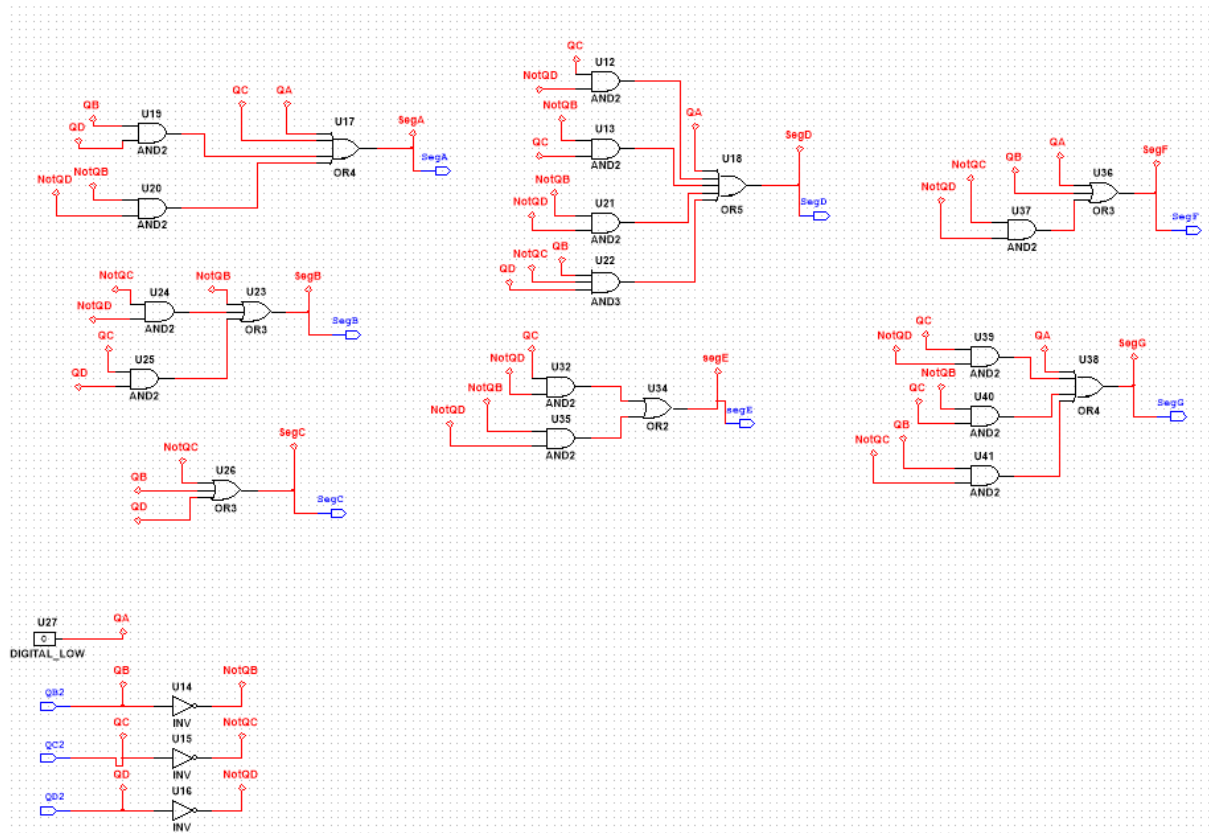


Figure 9 - Tens Decoder

This is the tens decoder circuit. This circuit is very similar to the units decoder but the difference being that QA will have a different connection.

Digital Stopwatch Testbed

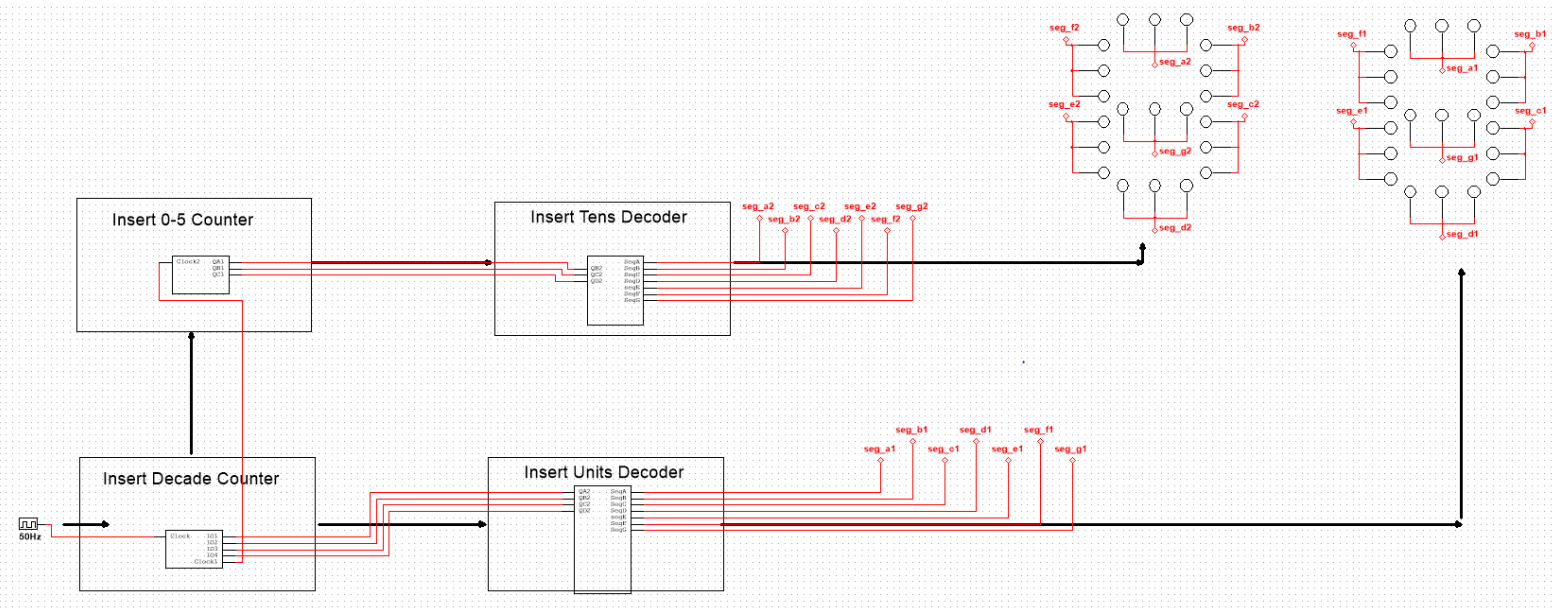


Figure 10 - Digital Stopwatch

Here is a screenshot of the final circuit. This circuit includes each individual circuit used as subscript circuits and then connected to one another. In order to do this there had to be input and output connectors placed inside the subscripted circuits.

NO RESULTS GRAPHS
SHOWN.

Analysis of Results

In order to do the simulation of the test for a digital stopwatch the package that was used was multisim. Each circuit then had to be constructed while being in PLD mode.

The first test that had to be done was the 0-5 counter circuit, this was tested by connecting the outputs to lights to see if the first figure would go through the sequence. As expected, the circuit was a success and was in good working order as each number from 0-5 lit up as they were supposed to.

The second test was very similar to the first one as it was to simulate the circuit but this time by using the 0-9 counter circuit. Again the circuit was also connected to lights and then put into simulation mode to see if the second figure would run the correct sequence. As expected, the circuit was a success and went through the 0-9 sequence correctly.

The Final test then was to combine the two circuits and then put them both into one simulation to see if they can create a 00-59 seconds stopwatch and then a clock was added and the speed was changed to 50 Hz. The results of this will be shown in the annex which is at the end of the report.

Conclusion

The results to the first test was good and gave all the correct reading and went through the correct sequence. At the start of this there was a little difficulty when the circuits had to be subscribed and then be connected to each individual segment. This problem was overcome by asking the lecturer how to subscript the circuits and connect them to each other, this was done by input and output connectors. The results from the second circuit was also correct and went through the sequence as it was supposed to.

When it came to the final test which was the combination of all four subscribed circuits with the digital stopwatch and its segments there was one issue that occurred during simulation and this was the speed of how fast the stopwatch was changing sequence. The cause of this was because the clock was running too slow through the sequence and therefore it was hard to take the readings and write down the results. The reason for this being that the clock was set to 1Hz, in order to rectify the problem the speed was increased by increasing the clock to 50Hz.

This report also helped when it came to fault finding on the simulated circuit as its different to a physical circuit. The reason of this is because the simulated circuit has calculated values and certain factors where as in a physical circuit there will have to be certain issues taken into consideration such as wire resistance.

One improvement that can be done for this assignment would be to create a physical circuit. The reason for this would be because it can show what the components look like, this will help with knowledge and understanding. Another advantage of this would be because it would show the deviation in the certain components that were used.

Bibliography

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Annexe for Supplementary Diagrams, Data Sheets and Large Results Tables etc.

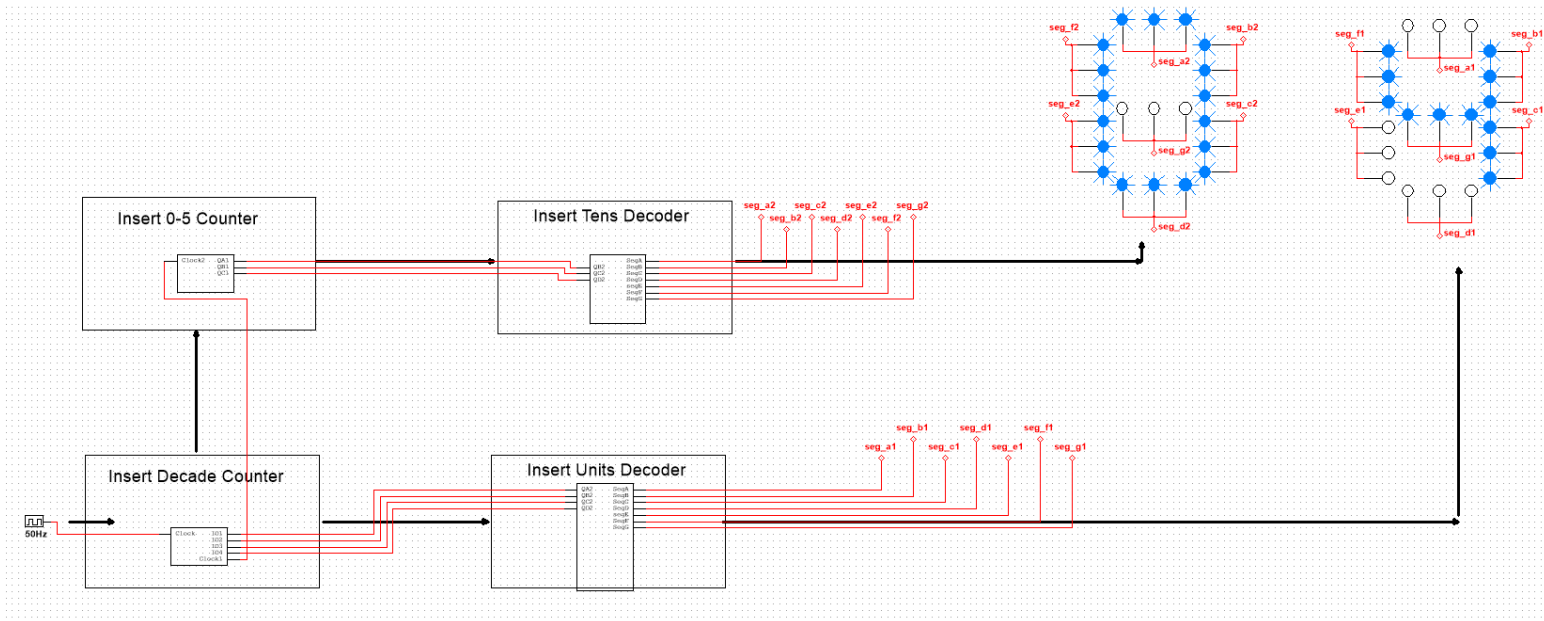


Figure 11 - Simulation Test 1

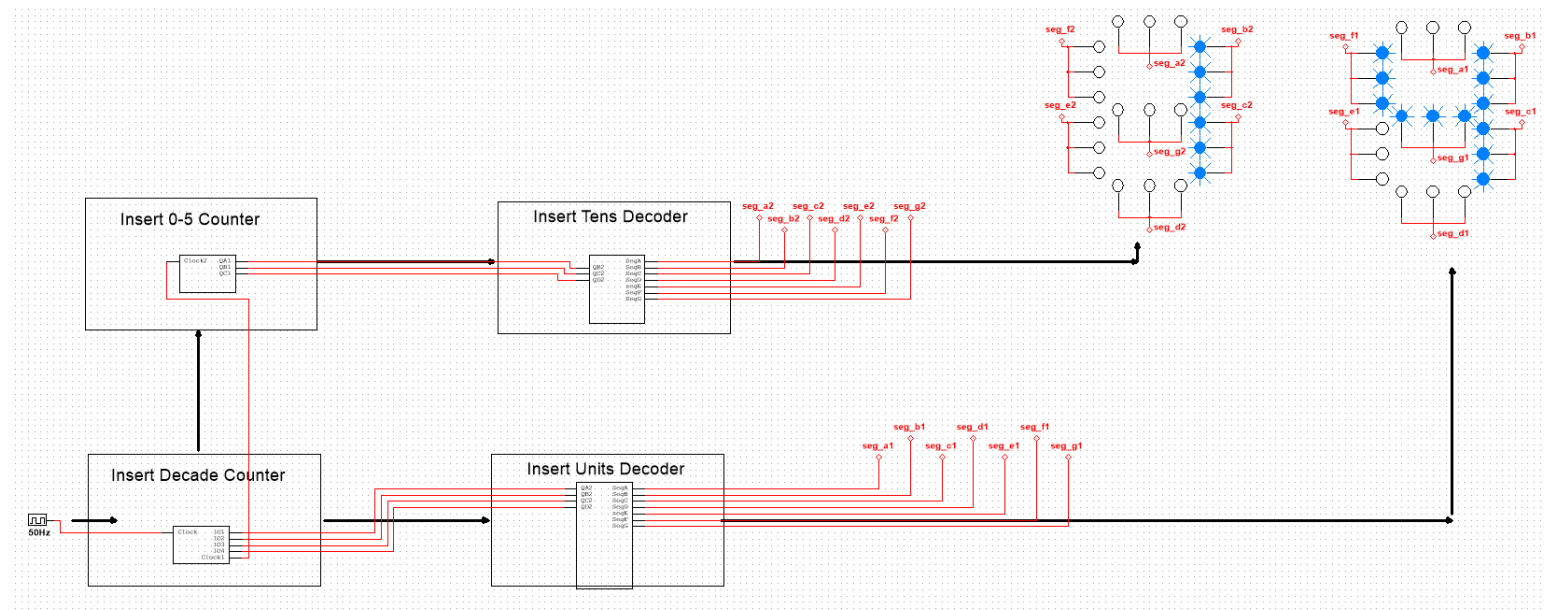


Figure 12 - Simulation Test 2

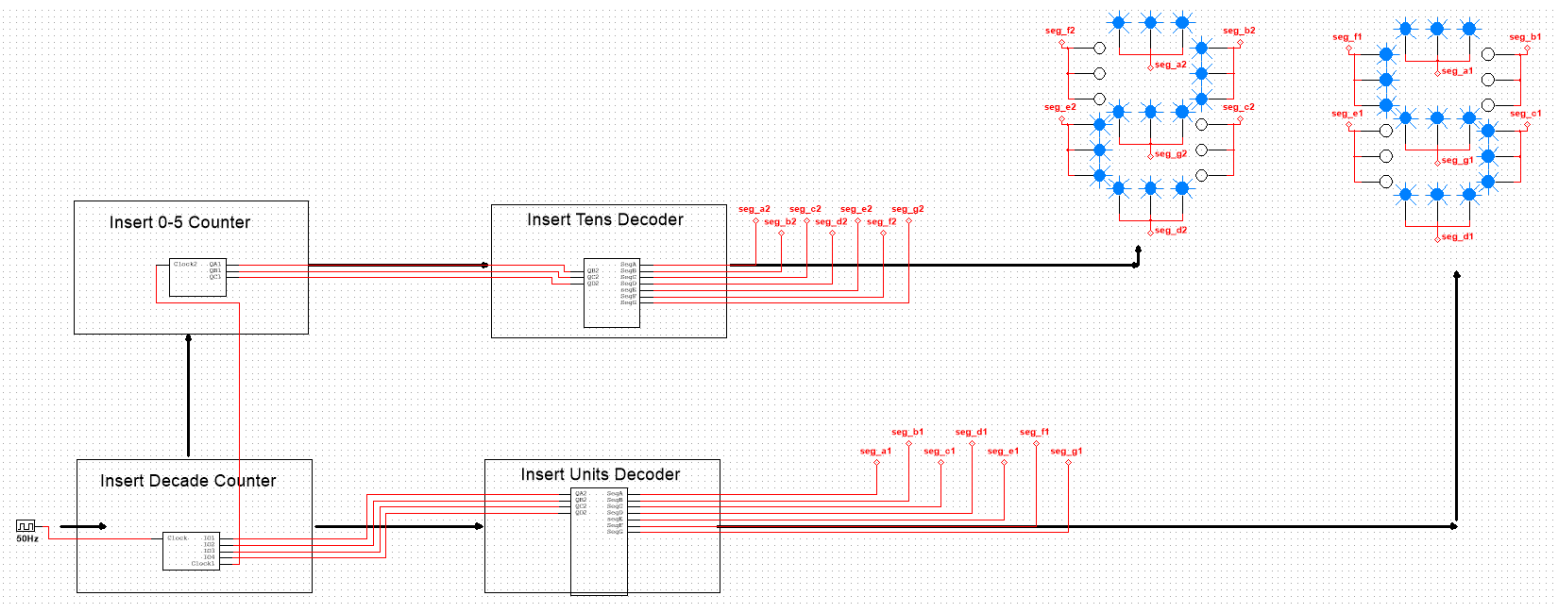


Figure 14 - Simulation Test 3

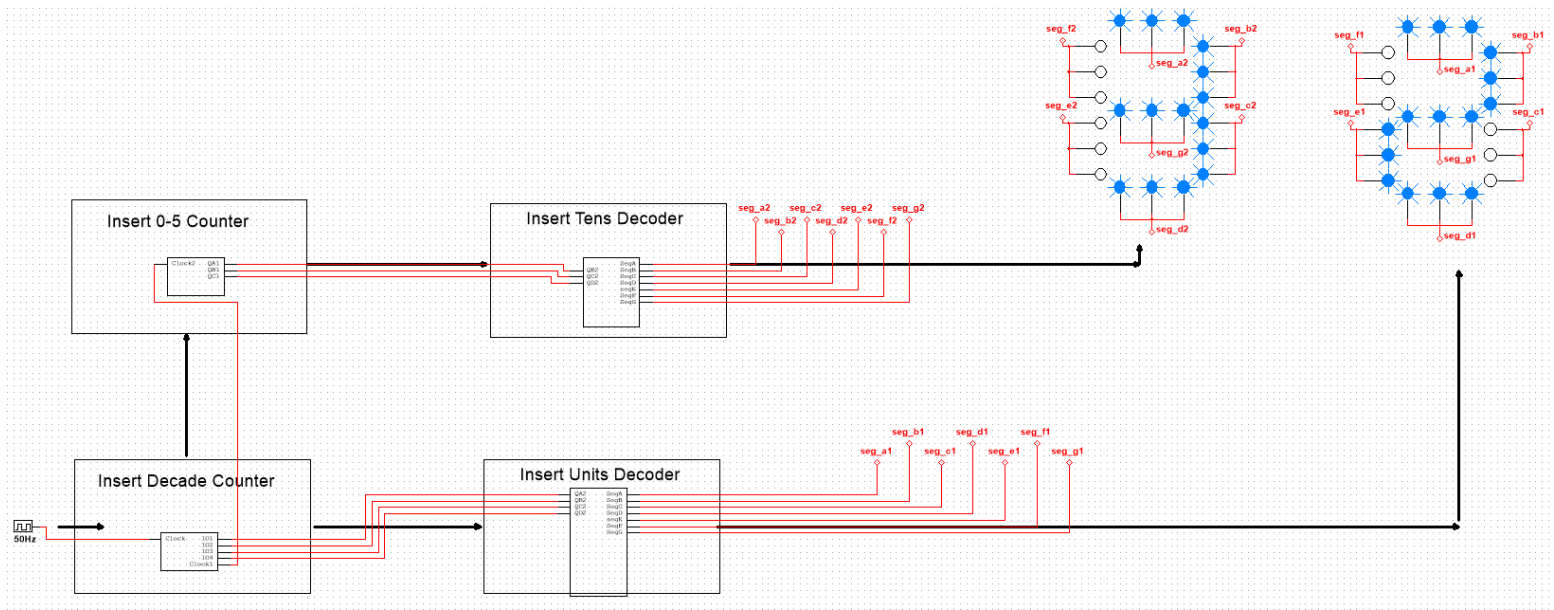


Figure 13 - Simulation Test 4

YOU NEEDED TO TEST THE
CIRCUITS USING A LOGIC
ANALYSER.

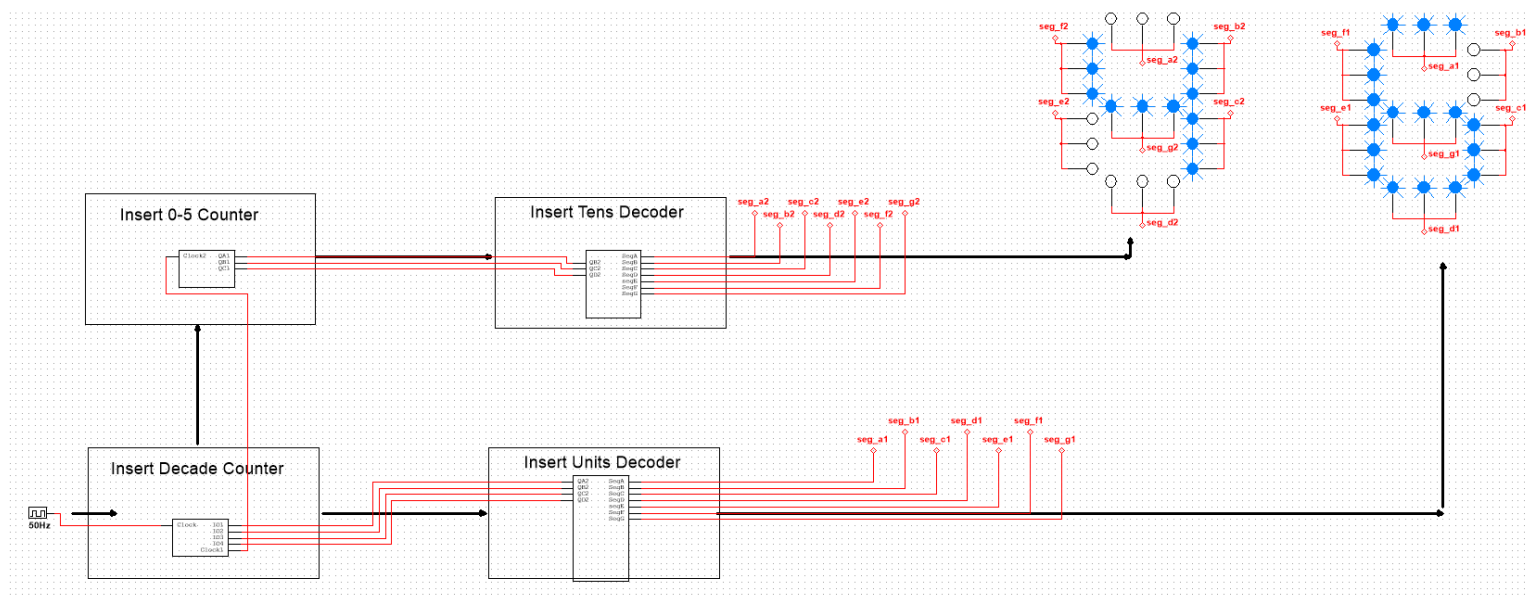


Figure 15 - Simulation Test 5

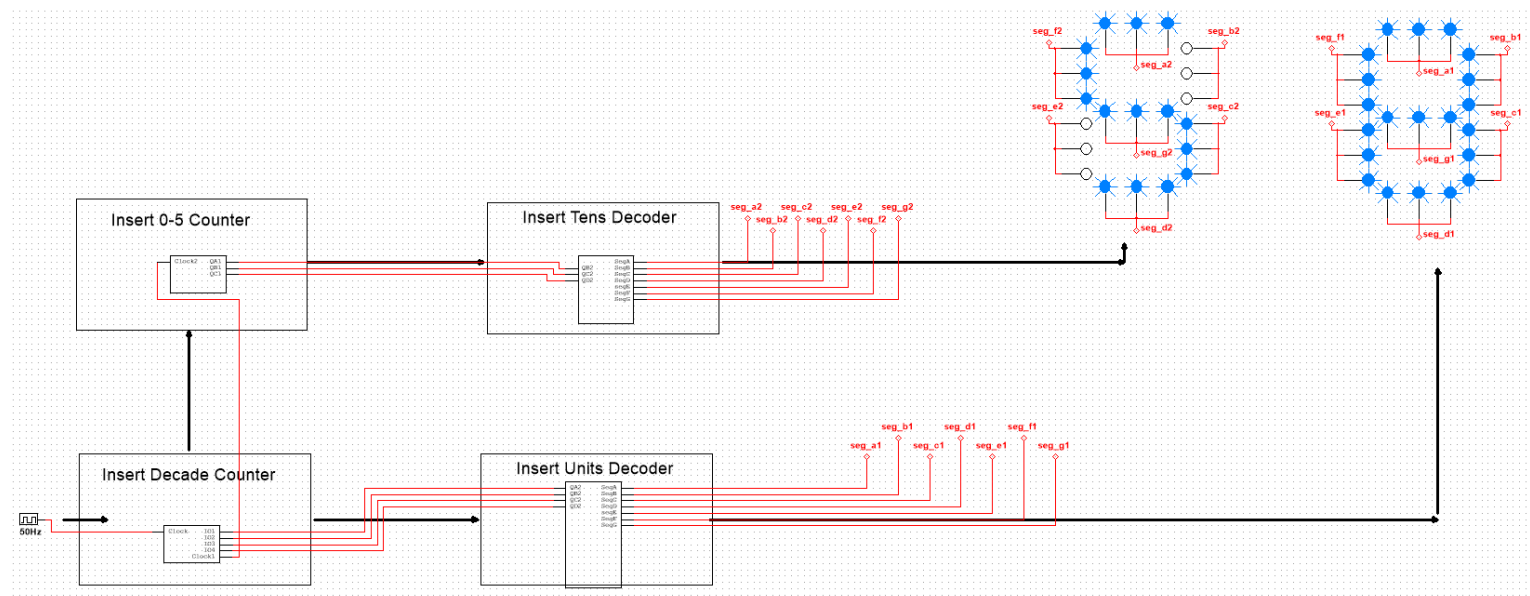


Figure 16 - Simulation Test 6

FINAL GRADE

GENERAL COMMENTS

Instructor

45/100

PAGE 1

PAGE 2

PAGE 3

PAGE 4

PAGE 5

PAGE 6

PAGE 7

PAGE 8

PAGE 9

PAGE 10

PAGE 11

PAGE 12

PAGE 13

PAGE 14

PAGE 15

PAGE 16

PAGE 17

PAGE 18

PAGE 19

GRADING FORM: CSG-RUBIC

JACK ROGERS**0****RESEARCH-INFORMED LITERATURE**

There was some evidence of further reading and research and your interpretation and understanding of the additional research was OK. The sources referenced were insufficient at this level given the amount of potential research areas for this assignment and relied on a small selection of mainly inappropriate and non-authoritative sources. You also need to include more in-text citations using the Harvard reference system.

4/10**KNOWLEDGE AND UNDERSTANDING**

The knowledge and understanding of the subject demonstrated by this assignment was reasonably detailed and mainly accurate. There were very few gaps in your knowledge of the basic concepts and your understanding of the higher level concepts was demonstrated to a limited degree - you could have explained in more detail how the circuit evolved. Further work – Your explanations need to

14/30

be more detailed and written with a greater emphasis on critical evaluation rather than description.

ANALYSIS



Your analysis of the task was mainly descriptive and superficial and lacked a lot of the required detail. Your conclusions were also mainly descriptive and there were several instances of flawed understanding. There was little evidence of critical analysis with most results accepted uncritically as fact and without explaining the underlying principles. You did however demonstrate some basic analytical skills and your approach to the task was logical.

12/30

PRACTICAL APPLICATION AND DEP.



The application of your practical skills for this task was generally rudimentary; you used the resources appropriately when designing the circuit and you used appropriate options for testing and evaluating the circuit performance - albeit to a limited fashion. Testing generally lacked a lot of the required detail however and you should have included a comprehensive set of results for each stage.

10/20

SKILLS FOR PROFESSIONAL PRAC.



In this assignment you have demonstrated skills in working individually and also collaboratively. Your

5/10

written report was generally good and contained most of the required detail, but was not written in a coherent and logical way. The available word count was under used.