

2017194

by Hefin Williams

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45-50

- ① RESEARCH IS OK WITH CORRECT CITATIONS, RANGE OF SOURCES COULD BE WIDER.
- ② THE EXPLANATION OF THE DESIGN WAS CONFUSING AND YOU MIXED UP THE TABLES, MAPS AND CIRCUITS OF THE 3 CIRCUITS. SOME TABLES AND MAPS WERE MISSING.
- ③ TESTING WAS CARRIED OUT, BUT AGAIN YOU MIXED UP THE CIRCUITS. IT WAS ALSO BASIC IN NATURE AND YOU SHOULD HAVE USED THE LOGIC ANALYSER MORE.
- ④ ANALYSIS WAS LIMITED AND AGAIN YOU MIXED UP THE CIRCUITS.
- ⑤ CONCLUSIONS WERE DESCRIPTIVE AND SHOULD BE MORE CRITICAL.

Executive Summary:

This report will investigate into assets of FPGA and ASIC semiconductor devices, application of a finite state machine as a design tool, alterations concerning sequential logic and combinational logic.

And to design, simulate, build, test and evaluate a digital stopwatch counting from 0 to 59 constantly. The circuit simulation, build and testing will be carried out via NI Multisim which is a circuit design software.

Introduction, aims and objectives:

Introduction:

This report will include a detailed and in-depth research with staggering evidence which will be sighted correspondingly. The report will have a detailed in depth understanding of the digital stopwatch counting from 0 to 59, the digital stopwatch will be presented in a professional manor.

Aims and Objectives:

The aims and objectives for this report is to show a advanced knowledge regarding a digital stopwatch which is using a Finite State Machine which will be instigated via NI Multisim in PLD mode.

All research in this report will be well presented and will be sighted correctly.

*Aims = WHAT
OBJECTIVES = HOW*

*SHOULD COVER ALL THE SECTIONS
OF THE REPORT AND DETAIL THE
MAIN FINDINGS.*

Research:

Alterations concerning Sequential Logic and Combinational Logic:

Combinational Logic:

Combinational logic as the name gives away is a combination of several logic gates. Regardless of time the output will always depend on the input terminals and not the past state inputs. This logic does not require any clocks or memory states as past inputs have no impact with the present state of the circuit. Regardless on the number of inputs feeding the circuit there will always be one individual output. (watelectronics, 2021)

Combinational logic is built up on three main functions Logic gates, Boolean Algebra and a truth table. Logic gates are what the combinational logic circuit is built up on which are AND, OR, NOT, NAND and NOR gates. The correlation between combinational logic and Boolean Algebra is Boolean variables that is used in the design of the digital circuit using logic gates. For generating a combinational logic circuit a truth table is used to calculate values of what the logic expressions must be according to their logical variables. When a combination logic circuit has one or more bit output each of the single bit output has a unique truth-table. (electronics-course, 2021)

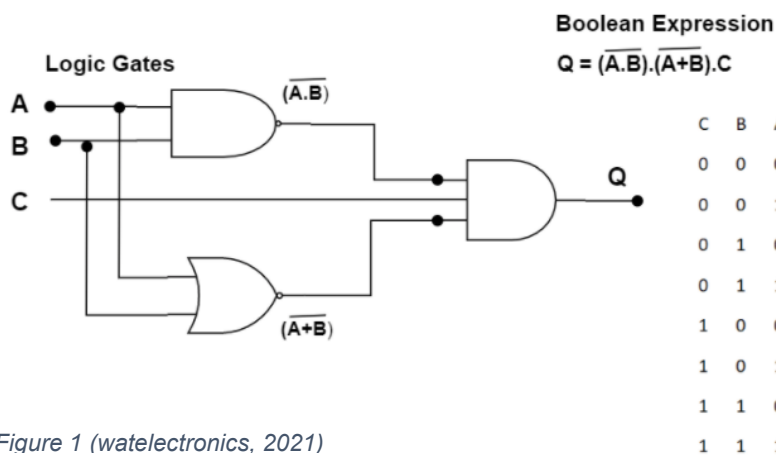


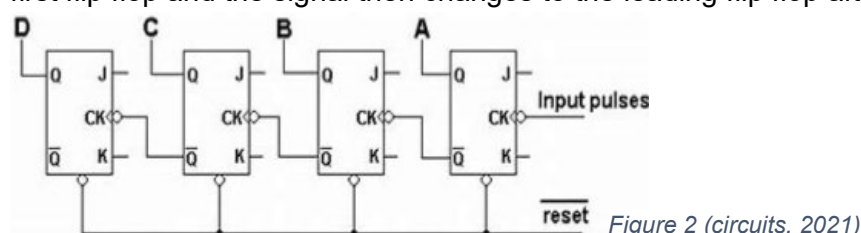
Figure 1 (watelectronics, 2021)

(Figure 1) shows a combinational logic circuit with all three main functions, the truth table showing the inputs as (A, B and C) and the output as (Q) this circuit will give a output when both inputs (B and A) are equal to=0 and input (C)=1. A Boolean expression has been generated according to the truth table. Then a

AND gate and a OR gate is used in the circuit calculated to give a combination of logic gates which is where the name combinational logic circuit comes from.

Sequential Logic:

Sequential logic circuits are centred on combinational logic circuits such as AND, OR, NOT, NAND and NOR gates. Sequential logic has registers built in the circuits which are made up of latches and flip-flops. (ScienceDirect, 2002) Sequential logic circuits give outputs concerning both the combination of logic states at its inputs and regarding the logic states that existed previous in the circuit. Then its dependent on the sequence of events that have and that are happening at the circuit inputs. (Learnaboutelectronics, 2021) Sequential logic circuits are uses in counters. Counters are registers that have a programmed sequence of clock pulses which is initially a finite state machine as its state diagram is one individual cycle. There are two kinds of counters asynchronous and synchronous counters. Synchronous counters is a clock signal which gives inputs to a flip flop which means every flip flop is allocated the same clock signal. Asynchronous counters is also a clock signal where the signal is now only at the first flip flop and the signal then changes to the leading flip flop afterwards. (elprocus, 2021)



Alterations:

Combinational logic circuits have no memory bits where on the other hand sequential logic circuits have flip flops which will give outputs regarding the previous inputs. Combinational logic circuits will give outputs dependant on the inputs whereas sequential logic circuits will give a output considering the previous and current input.

Finite State Machine as a design tool:

A finite state machine is a machine that calculates inputs, it's a theoretical tool that is used to process a given sequence to change a state of the system. After all inputs have been processed the machine will perceive the final state in order to control whether or not the input sequence is accepted. A finite state machine of the following components; States, Initial state, Accepting state and transitions. State is a finite sum of states that the system can be in at one given time, and is symbolised in (Figure 3) below. Initial state is the initial start up of the system which is symbolised in (Figure 4) below. Accepting states is a compartment of states that is known to the machine where the machine will decide if the input processed is valid, the symbol for this is shown on (Figure 5) below. Alphabet is the language set for each of the valid inputs. Transitions is the process the machine will go through when deciding how the machine will move from a initial state to another, the symbol for transitions is shown in (Figure 6) below.

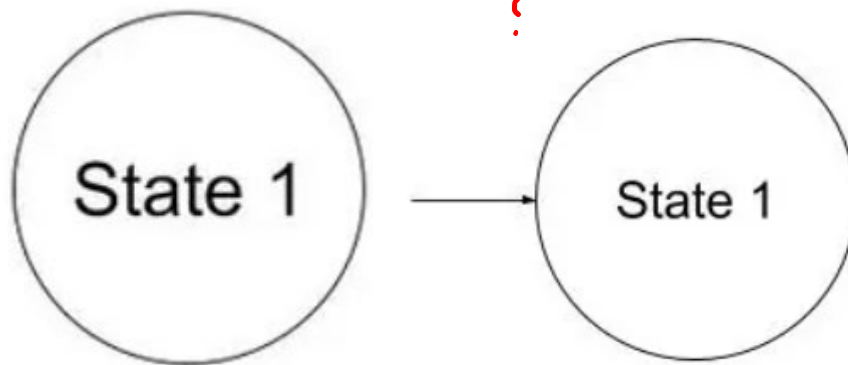


Figure 3 (Abuse, 2021)

Figure 4 (Abuse, 2021)

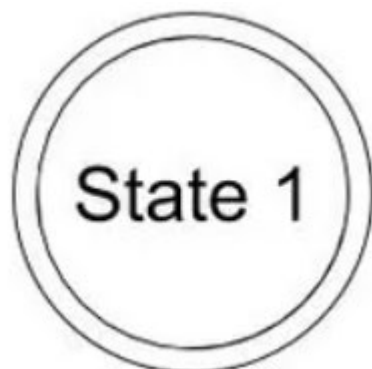


Figure 5 (Abuse, 2021)

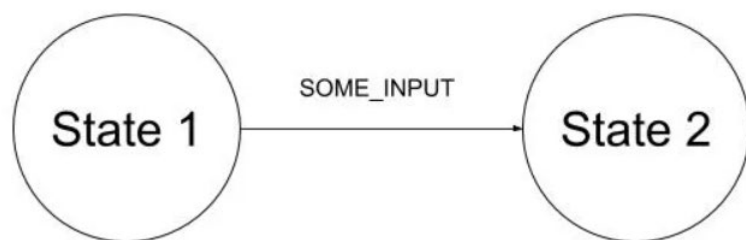


Figure 6 (Abuse, 2021)

JUST 1 CITATION
WILL SURVE.

The assets of FPGA and ASIC:

FPGA:

Field Programmable Gateway Arrays are semiconductors which are small micro chips which do as it suggests in the name, gate arrays that are arranged in a certain way as the designer wants. Within the chip there are many logic blocks which are programmable to whatever the designer demands the chip to do. (Hardwarebee, 2021).

ASIC:

Application Specific Integrated Circuit is a microchip which is specially designed for one specific function. There are two different designs for an ASIC chip for specific activities to take place in a device. The two different means are full custom and gate array design. (Smith, 2021).

Assets of both FPGA and ASIC:

The performance of a FPGA is that they can process and do calculations in a rapid rate compared to a general CPU, regardless to the fast processing speed the ASIC chip is processing speed is much faster as it does not have additional wiring and gates inside of them. The programmability of both chips are limited but a ASIC chip can not be modified after production different to the FPGA chip where its code can be easily updated and changed in the field with its new function. The cost of the FPGA chip is proven to be very cost effective as it can be re coded more than once. A ASIC chip is cheaper upon purchase but in the long run where the chip will have to have new hardware and be redesigned the FPGA chip is evidently more cost effective. When it comes to prototyping the FPGA chip is the best as they are reusable which makes them the best choice in order for prototyping. ASIC chips would not be efficient when it comes to prototyping as if there's one adjustment needed the whole chip would have to be scrapped. (Hardwarebee, 2021)

SOME GOOD RESEARCH.

Design Method:

Designing a digital stopwatch that will count 00 to 59 continuously. The design of the stopwatch was designed using a finite state machine which was then applied on NI Multisim in PLD mode.

Firstly, a truth table is generated with the current states and the next states that will be included in the finite state machine. This truth table is used to draw the 7 segment counter. The truth table is shown in (Table 1) below.

Current	Next+	Current				Next+			
		Qa	Qb	Qc	Qd	Qa+	Qb+	Qc+	Qd+
S0	S1	0	0	0	0	0	0	0	1
S1	S2	0	0	0	1	0	0	1	0
S2	S3	0	0	1	0	0	0	1	1
S3	S4	0	0	1	1	0	1	0	0
S4	S5	0	1	0	0	0	1	0	1
S5	S6	0	1	0	1	0	1	1	0
S6	S7	0	1	1	0	0	1	1	1
S7	S8	0	1	1	1	1	0	0	0
S8	S9	1	0	0	0	1	0	0	1
S9	S0	1	0	0	1	0	0	0	0
S10	X	1	0	1	0	X	X	X	X
S11	X	1	0	1	1	X	X	X	X
S12	X	1	1	0	0	X	X	X	X
S13	X	1	1	0	1	X	X	X	X
S14	X	1	1	1	0	X	X	X	X
S15	X	1	1	1	1	X	X	X	X

Table 1

The truth table above was used to generate these Karnaugh maps shown in (Figure 7) below.



Figure 7

YOU HAVE THE TRUTH TABLE FOR THE DECADE COUNTER, BUT THE MAPS OF THE 7 SEGMENT DECODER

0-5 counter.

Shown below in (Table 2) is the truth table drawn for the start design for the decade counter.

Present State	Next Stage	Present			Next State		
		Qa	Qb	Qc	Qa+	Qb+	Qc+
S0	S1	0	0	0	0	0	1
S1	S2	0	0	1	0	1	0
S2	S3	0	1	0	0	1	1
S3	S4	0	1	1	1	0	0
S4	S5	1	0	0	1	0	1
S5	S0	1	0	1	0	0	0
S6	x	1	1	0	x	x	x
S7	x	1	1	1	x	x	x

Table 2

Below in (Figure 8) is the Karnaugh maps drawn for the decade counter the values were gathered from the truth table shown in (Table 2).

	00	01	11	10
00	0	0	1	0
01	1	0	x	x

$$Q_A^+ = ?$$

	00	01	11	10
00	0	1	0	1
01	0	0	x	x

$$Q_B^+ = ?$$

	00	01	11	10
00	1	0	0	1
01	1	0	x	x

Figure 8

After generating the Karnaugh maps shown in both (Figure7) and (Figure 8) Boolean expressions were generated before building the circuit on Multisim.

$$Q_C^+ = ?$$

DELODER.

Shown below in (Figure 9) is the circuit generated for the 7 segment counter. The circuit was built Via NI Multisim.

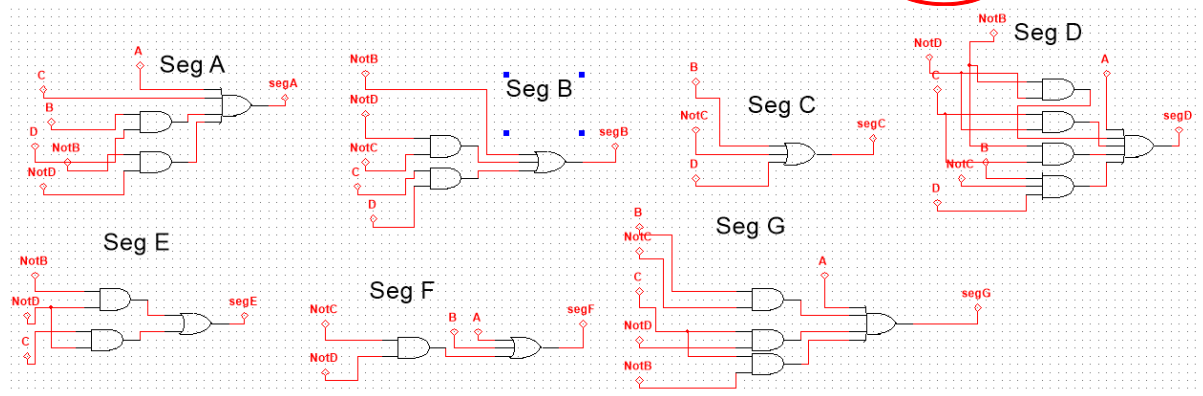


Figure 9

Shown below in (Figure 10) is the circuit generated for the decade counter. The circuit was built Via NI Multisim.

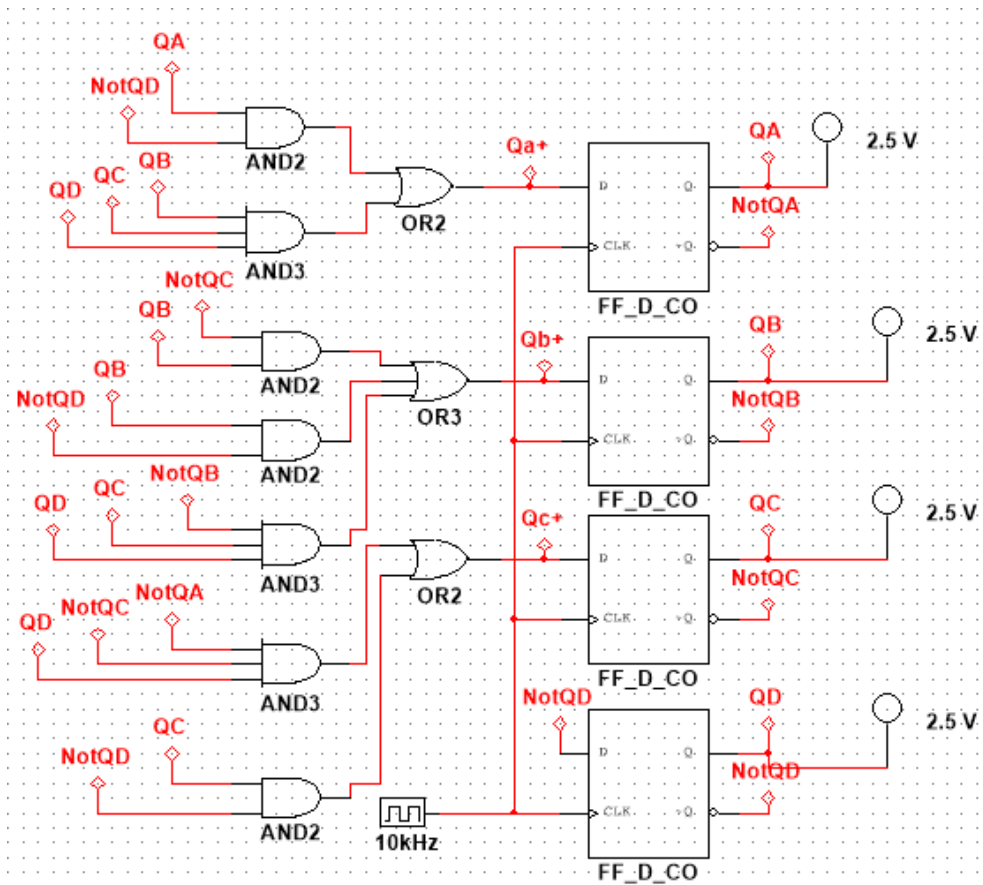


Figure 10

Simulation testing, Analysis of results:

The testing of the 7-segment counter was carried out on Multisim and had LED probes as the display shown in (Figure 11) below.

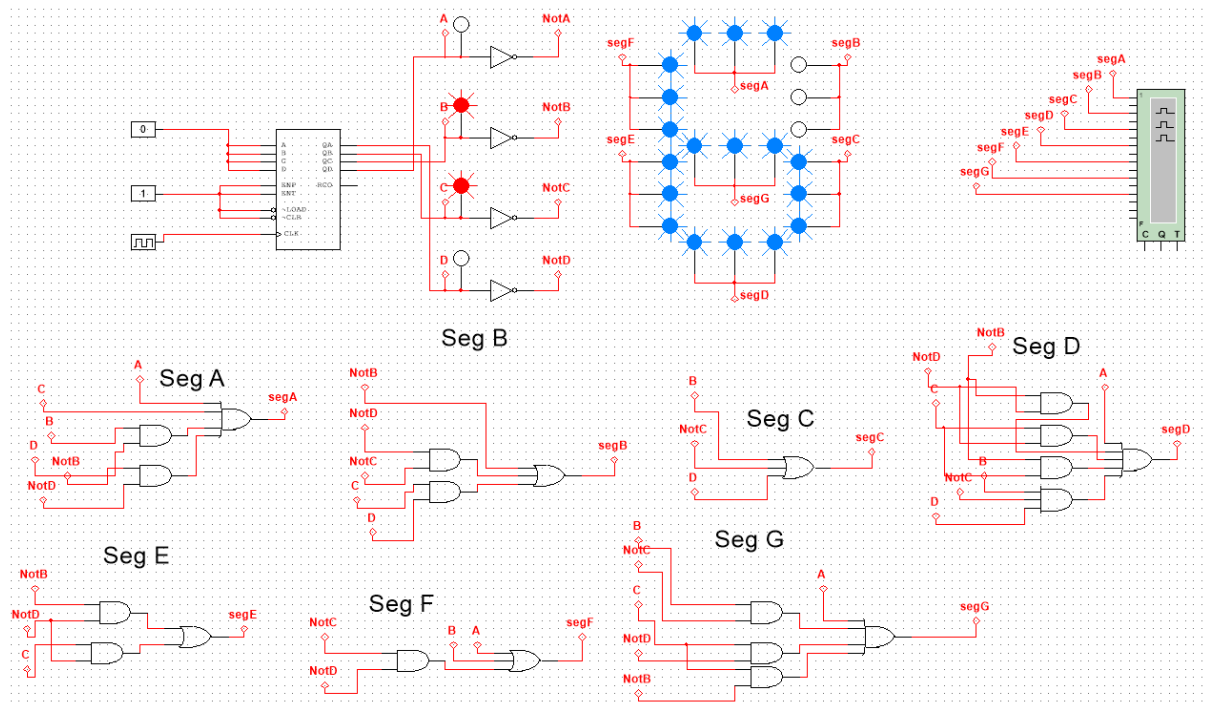


Figure 11

In order to test the circuit shown in (Figure 9) the circuit was added to a 0-59 count display screen as a sub screen shown in (Figure 12).

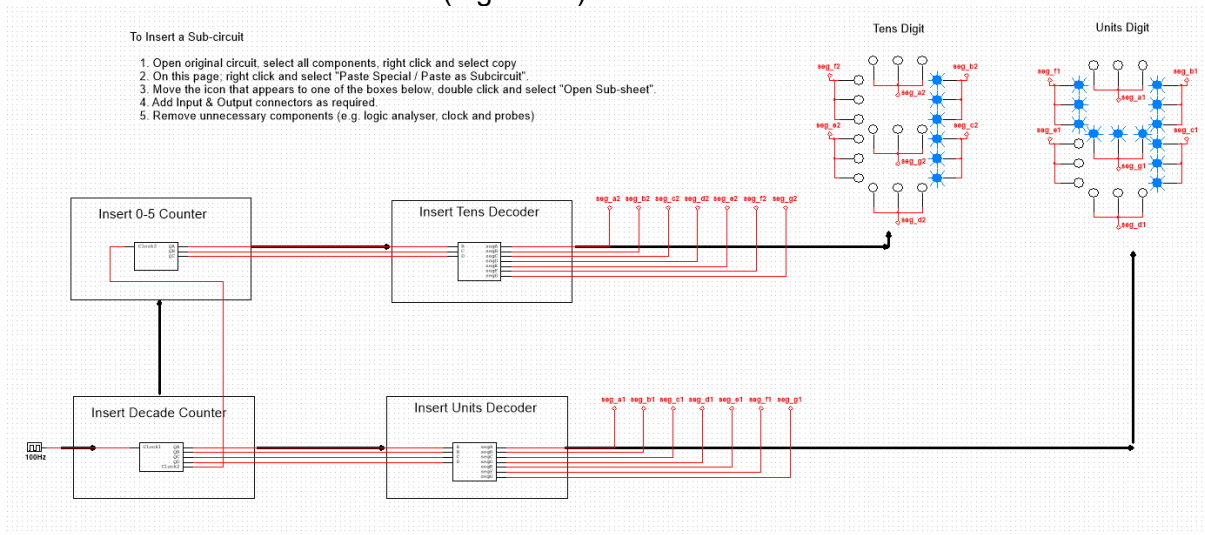
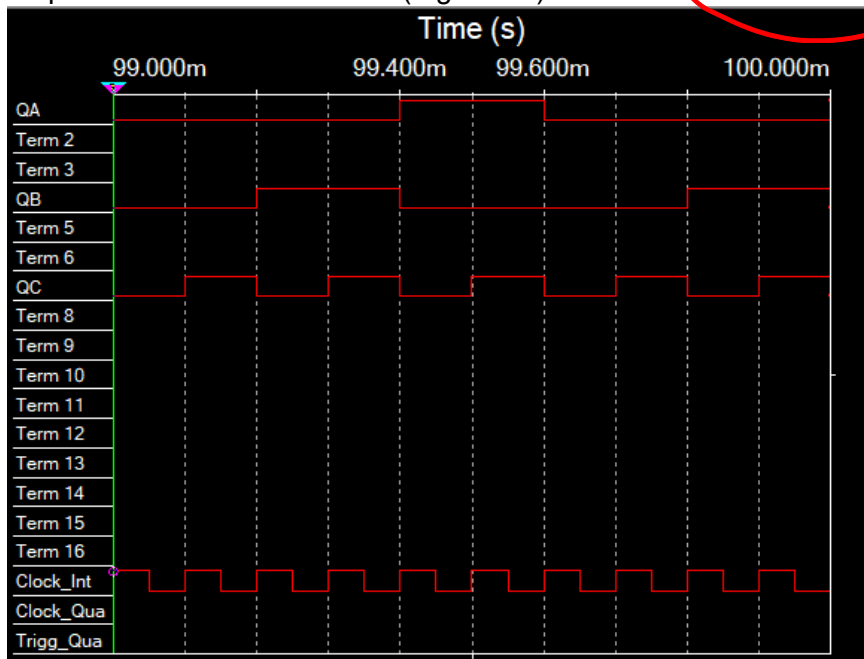


Figure 12

Shown in (Figure 13) below is a screen shot of the logic analyser which shows the logic outputs of the circuit shown in (Figure 10) which is the decade counter.

0-5 counter.



*USE REVERSE FOR
A WHITE BACKGROUND*

Figure 13

Shown in (Figure 14) below is a screen shot of the logic analyser which shows the logic outputs of the circuit shown in (Figure 11) which is the seven-segment counter.

*DECADE
COUNTER.*

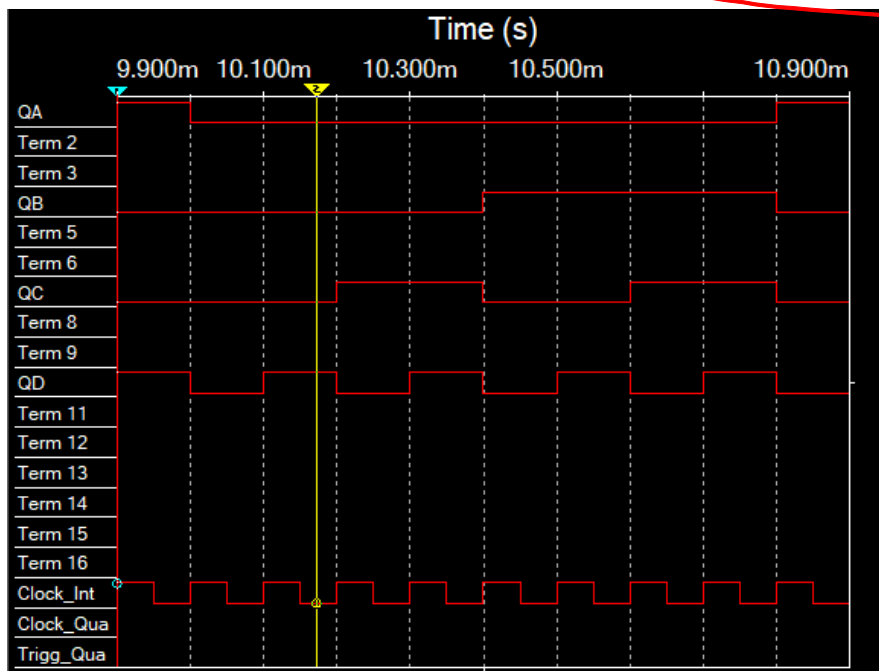


Figure 14

(Figure 15) below is the final simulated test to be carried out on the circuits all grouped together on one Multisim screen with a display of 59.

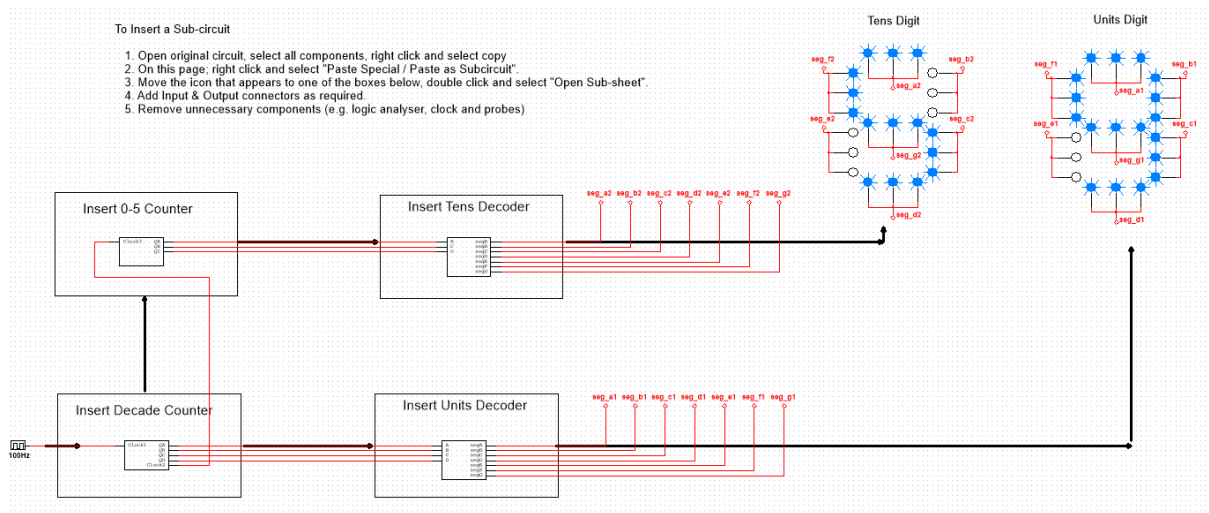


Figure 15

Conclusion:

In conclusion this report has covered background research regarding the difference between combinational and sequential logic, the use of Finite state machine as a design tool also the assets of both FPGA and ASIC chips. The design, simulate, build and test of the 00 to 59 second digital stopwatch was a complete success. A thorough understanding and explanation of how each step of the stopwatch was made also how each circuit were tested. The stopwatch was able to count from 00 to 59 seconds with no trouble whatsoever. The results found whilst doing each test were as follows; When testing the seven segments counter in (Figure 11) the results were as expected whereas the circuit was simulated in run mode the 7-segment display would give a count of 0-9, (Figure 11) captured the circuit at a count of 6 where the LED indicated a binary code of 0110 which proves the Karnaugh maps correct. Testing of the decade counter is shown in (Figure 12) where each of the circuits were built into singular chips and were run all together to see whether the final circuit worked all linked together, the results found were successful with the stopwatch counting from 00-59 two screen shots were taken where the count was captured at 59 in (Figure 15) and a count of 14 in (Figure 12). A logic analyser was added to the 7-segment counter to analyse the logic outputs of the circuit, the results are shown in (Figure 14) where the code was captured showing 0001. A logic analyser was also added to the decade counter in order to visualise the decade counter output as a given time, the screenshot is shown in (Figure 13) where the code output of the circuit is captured as 0001 yet again. The design of the digital stopwatch was using combinational logic circuits as all outputs were dependant on a current input regardless of the time. A different approach could have been to use sequential logic where the outputs would be affected not only by the current inputs but also by present inputs also.

*MORE OF A NARRATIVE THAN A
CONCLUSION.*

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FINAL GRADE

GENERAL COMMENTS

Instructor

48/100

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GRADING FORM: CSG-RUBIC

HEFIN WILLIAMS

0

RESEARCH-INFORMED LITERATURE

 There was evidence of further reading and research and some in text referencing. Your references were mainly appropriate to the task, however the reference list was short and you should increase the breadth of your research for future assignments. There was a heavy reliance on information gained from the course notes.

5/10

KNOWLEDGE AND UNDERSTANDING

 The knowledge and understanding of the subject demonstrated by this assignment was generally adequate. The circuits worked and the explanation of how this was achieved was included, but only to a descriptive level, there was little evidence of any critical understanding. Your report lacked depth and detail at times and didn't really extend your knowledge beyond that contained in the course notes. Further work – Research results need to be in much more detail and written in a more logical and clearer way.

15/30

ANALYSIS



Your analysis of the task was generally satisfactory, both in class and as shown in this assignment, however it did tend more towards descriptive rather than analytical. You have demonstrated some analytical skills and your approach to the task was logical. You wrote a short conclusion that demonstrated some skills in analysing quantitative and qualitative data, however this was generally basic in nature. Further work – in your conclusion, you should relate the results to the original specification and to accepted theory and provide a detailed critical analysis of this.

12/30

PRACTICAL APPLICATION AND DEP.



The application of your practical skills for this task was generally rudimentary; you used the resources appropriately when designing the circuit and you used appropriate options for testing and evaluating the circuit performance - albeit to a limited fashion. Testing generally lacked a lot of the required detail however and you should have included a comprehensive set of results for each stage.

10/20

SKILLS FOR PROFESSIONAL PRAC.



Your written report was reasonably well presented in terms of content and layout, but was not written in a coherent and logical way. You should also endeavour to use the available word count more effectively in future.

6/10