

SURNAME: Butler

FORENAME(S): Sarah.

2315177

12 Pages

1. Please give the information requested in the boxes below.
2. Enter your name in the space provided to the right, fold over and seal down (using the label provided) to hide your name.
3. The answers must be legibly written. The Examiners can either ignore illegible script or have it typed and the expense of typing charged to the candidate.
4. Write your answers in ink.
5. Begin each answer on a fresh page. Do all rough work in the answer book and cross it through.
6. No part of this book is to be torn out; it must be handed in complete.
7. If more books than one are used, fasten them together using the tags available from the invigilator(s).
8. **Every book must be handed in. In no circumstances may answer books, used or unused, be taken out of the examination venue.**

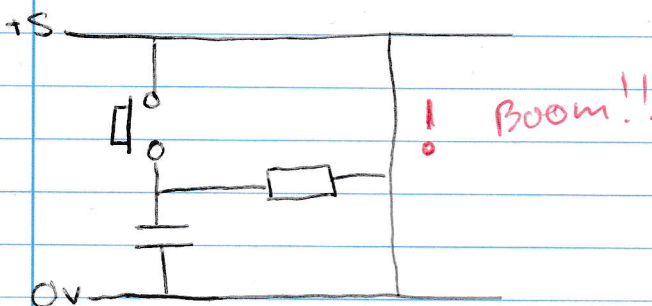
7	Number of Answer Books handed in	ONE
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List the numbers of the questions you have attempted	Office Use
1	6
2	4
3	3
4	10
5	8
6	4
	35
Total	70%

$$\begin{array}{r} 6 \\ 4 \\ 3 \\ 10 \\ 8 \\ 4 \\ \hline 35 \end{array}$$

- 1a Return from subroutine - used at the end of a subroutine to resume main code next operation $1\frac{1}{2}$ $1\frac{1}{2}$
- 1b Sleep - standby for new operation 0
- 1c add L with W - add literal value (a constant) to the value in working register 2 2
- 1d bit clear F, b - bit clear the file 'f', all bits to zero $\frac{1}{2}$ $\frac{1}{2}$
- 1e decrement F - decrement one from the value in file f 2 $\frac{2}{6}$

2 One way to reduce switch bounce in a circuit is to use an RC circuit, as the RC filters - makes an RC time constant which smooths



Another way to reduce switch bounce is to use a schmitt trigger. This has two thresholds, one for when transitioning low to high voltage and another for high to low. The difference between the thresholds is called 'hysteresis'.

2 cont. Hysteresis makes it so that when either threshold is crossed, it is difficult to return - which reduces switch bounce



2

2

4

3

AND gate



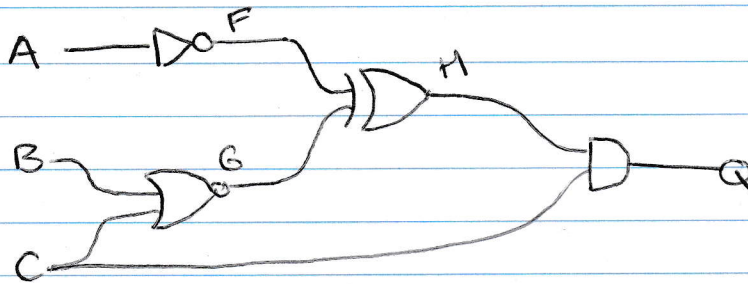
Truth table

A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

3

3

4

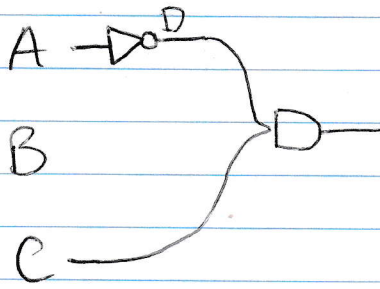


A	B	C	F	G	H	Q
0	0	0	1	1	0	0
0	0	1	1	0	1	1
0	1	0	1	0	1	0
0	1	1	1	0	1	1
1	0	0	0	1	1	0
1	0	1	0	0	0	0
1	1	0	0	0	0	0
1	1	1	0	0	0	0

7

7

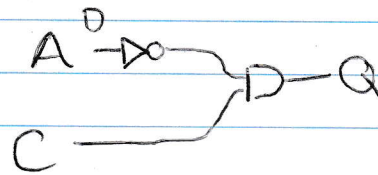
4 cont.



Output:

A	B	C	Q
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

A	B	C	D	Q	C & A'
0	0	0	1	0	
0	0	1	1	1	
0	1	0	1	0	
0	1	1	1	1	
1	0	0	0	0	
1	0	1	0	0	
1	1	0	0	0	
1	1	1	0	0	

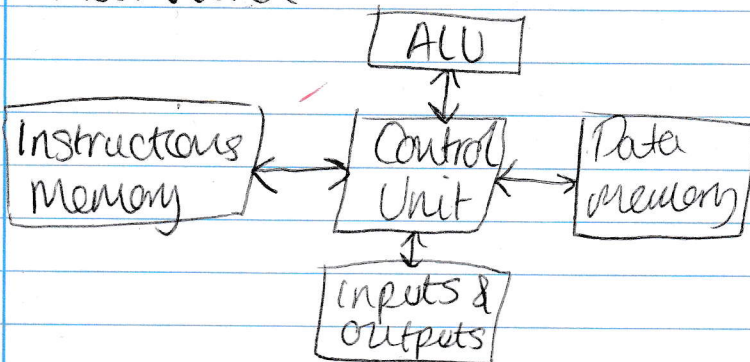


3

3

10

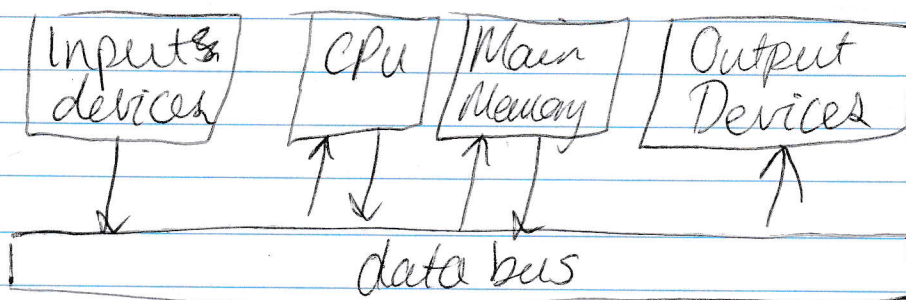
5 Harvard:



4

4

Von Neumann:



2

2

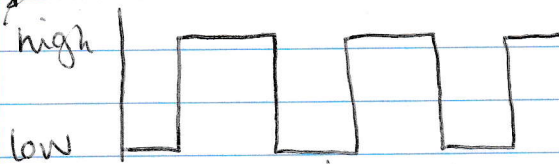
Cont. the Harvard processor architecture has separate memory for data and instructions. This means it is more efficient as it can fetch both instructions and data simultaneously. ✓

The Von Neumann processor architecture is more simple and less expensive than the Harvard architecture. This means it is used for more general purpose computing. ✓

6 PWM is pulse width modulation. This controls the power that is given to a circuit - dependant on the duty cycle. The duty cycle is the percentage of high pulses. A 100% duty cycle means it is always on and power is fully transferred. A 0% duty cycle means that it is always off and no power is transferred. 4

A DAC is a digital to analog converter which converts a digital voltage into an analog signal.

B PWM:



PWM signal (50% duty cycle)