

12 Pages

1. Please give the information requested in the boxes below.
2. Enter your name in the space provided to the right, fold over and seal down (using the label provided) to hide your name.
3. The answers must be legibly written. The Examiners can either ignore illegible script or have it typed and the expense of typing charged to the candidate.
4. Write your answers in ink.
5. Begin each answer on a fresh page. Do all rough work in the answer book and cross it through.
6. No part of this book is to be torn out; it must be handed in complete.
7. If more books than one are used, fasten them together using the tags available from the invigilator(s).
8. **Every book must be handed in. In no circumstances may answer books, used or unused, be taken out of the examination venue.**

List the numbers of the questions you have attempted	Office Use
1	21 ^{1/2}
2	25
4	1
5.	0
Total	47 ^{1/2}

(Gweler yr ochr arall am y fersiwn Cymraeg)

FORENAME(S): SEAN MATTHEW.

MARK
Agree
48%



Prifysgol Cymru
Y Prifod Dewi Sant
University of Wales
Trinity Saint David

Cyfarwyddiadau i Ymgeiswyr

12 Tudalen

ENW(AU) CYNTAF:

CYFENN:

Llenwch, plynwch a seliwch
(gweler nodyn 2 isod)

1. Rhwch yr holl wybodaeth y gofynnir amdani yn y blychau isod.
2. Rhwch eich enw yn y lle a ddarparwyd ar y dde, plynwch ef a'i selio i lawr (gan ddefnyddio'r label a ddarparwyd) i guddio'ch enw.

3. Rhaid i'r atebion fod mewn llawysgrifen ddal, gael ei theipio a chael yr ymgeisydd i dalu.

4. Ysgrifennwch eich atebion mewn inc.

5. Dechreuwch bob ateb ar dudalen newydd. Gwnewch unrhyw fras nodiadau yn y llyfr atebion a thynnu llinell drwyddynt.

6. Ni ddylid rhwygo unrhyw ran o'r llytr hwn; rhaid ei gyflwyno yn gyfan.

7. Os defnyddir mwy nag un llyfr, rhwymwch hwy gyda'i gilydd gan ddefnyddio'r tagiau sydd ar gael oddi wrth y gwyllwrr/gwyllwyr.

8. Rhaid dychwelyd pob llyfr. Ni chaniateir mynd â llyfrau atebion, wedi eu defnyddio neu heb eu defnyddio, allan o'r lleoliad arholi o dan unrhyw amgylchiadau.

7	Nifer y Llyfrau Atebion a gyflwynwyd	
6	Rhif Sedd	
5	Lleoliad yr Arholiad	
4	Dyddiad ac Amser yr Archoliad	
3	Cod y Modwl	
2	Teitl y Papur Arholiad	
1	Rhif Myfyrwr	

(See the other side for English version)

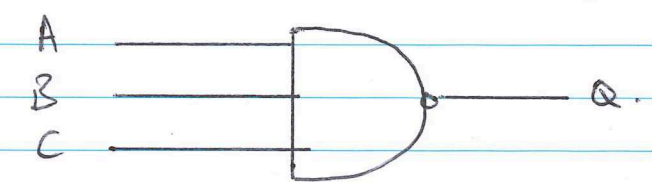
Rheswch ffau'r cwestiynau a ymgeistwyd gennyh	
At Ddibenion y Swyddfa	

Question 1.

(a) Auto test function and reduced fault detection ^{test} sequence is broadly the function and purpose.
These methods are used for complex digital systems and are implemented using a set of simple rules for individual logic gates. Reduced test sequence ✓
are derived by eliminating redundant test vectors ✓
and are further reduced by the use of wild cards ✓
to create and eliminate redundant test vectors. ✓

3

(b) NAND. (3 input).

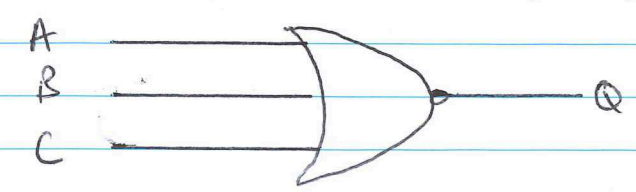


Test No.	A	B	C	Q.
1	1	1	1	0
2	0	1	1	1
3	1	0	1	1
4	1	1	0	1

2

2

NOR. (3 input). This only needs 2 ipr!



Test No.	A	B	C	Q.
1	<u>0</u>	<u>0</u>	0	<u>1</u>
2	<u>1</u>	<u>0</u>	0	<u>0</u>
3	<u>0</u>	<u>1</u>	0	<u>0</u>
4	0	0	1	0

✓

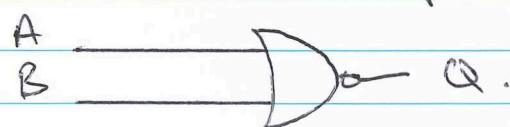
Question 1.

(b) Continued.

As with the case with the NAND gate, logic 0 is the unique logic function. 4 tests are carried out to satisfy the equation $m+1$ although it is a 3 input NAND gate.

As with the NOR gate, logic 1 is the unique logic function. As seen below 3 tests were carried out to satisfy the equation $m+1$ although it is a 2 input NOR gate.

NOR - Two input.



Test No.	A	B	Q.
1	0	0	1
2	1	0	0
3	0	1	0

As with the NAND gate, for any low input, for example a logic 0 it will produce a logic 1 on the output node Q.

As with the NOR gate, for any high input, for example a logic 1 it will produce a logic 0 on the output node Q.

Far more here than necessary.

Question 1.

(c)

As for figure 1a,

As for node Z, all inputs, A, B and C to the NAND gate are set to logic 1. All inputs D, E to the NOR gate are set to logic 0. This would be the case for a no fault condition.

Node F does not matter at this point as it only effects output node Q good.

The output for the NAND gate will be logic 0.

The output for the NOR gate will be logic 1.

If any of the inputs to the NAND gate were set low, for example logic 0 then this will effect the condition of node Z at the output. Node Z will be effected via the AND gate. As a result the output node Q good will detect an error or fault.

In this case node X will be logic 1. This will effect node Z at the output via the AND gate.

As a result there will be a stuck at fault created where inputs A, B and C STA 0 and X STA 1. This is the stuck at fault created.

Any logic 0 at the input of the NAND gate will produce a STA 1 fault at the output of the NAND gate, in this case node X.

This will then produce a fault at node Z via the AND gate and a fault or error will be detected at output node Q good.

Question 1.

(d)

Test Pattern.

(i)

A	B	C	D	E	F	A+	B+	C+	D+	E+	F+
1	1	1	0	0	0	0	1	1	0	0	0
0	1	1	0	0	0	1	0	1	0	0	0
1	0	1	0	0	0	1	1	0	0	0	0
1	1	0	0	0	0	0	0	0	1	0	0
0	0	0	1	0	0	0	0	0	0	1	0
0	0	0	0	1	0	1	1	1	1	1	0
1	1	1	1	1	0	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	0	0	0

 $\frac{1}{2}$

②

A+

DEF	ABC	000	001	011	010	100	101	111	110
000	0	0	1	0	0	1	0	0	0
001	0	0	0	0	0	0	0	0	0
011	0	0	0	0	0	0	0	0	0
010	1	0	0	0	0	0	0	0	0
100	0	0	0	0	0	0	0	0	0
101	0	0	0	0	0	0	0	0	0
111	0	0	0	0	0	0	1	0	0
110	0	0	0	0	0	0	1	0	0

 $\frac{1}{2}$

①

$$A+ = DA-$$

$$A+ = NA.NB.NC.ND.E.NF + NA.B.C.ND.NE.NF + A.NB.C.ND.NE.NF + A.B.C.D.E.F + A.B.C.D.E.NF$$

$\times$ grouping not taken into account!

 $\frac{1}{2}$

B+

DEF	ABC	000	001	011	010	100	101	111	110
000	0	0	0	0	0	1	1	0	0
001	0	0	0	0	0	0	0	0	0
011	0	0	0	0	0	0	0	0	0
010	1	0	0	0	0	0	0	0	0
100	0	0	0	0	0	0	0	0	0
101	0	0	0	0	0	0	0	0	0
111	0	0	0	0	0	0	1	0	0
110	0	0	0	0	0	0	1	0	0

 $\frac{1}{2}$ $\frac{1}{2}$

$$B+ = DB-$$

$$B+ = NA.NB.NC.ND.E.NF + A.NB.C.ND.NE.NF + A.B.C.ND.NE.NF + A.B.C.D.E.F + A.B.C.D.E.NF$$

C+

DEF	ABC	000	001	011	010	100	101	111	110
000	0	0	1	0	0	0	1	0	0
001	0	0	0	0	0	0	0	0	0
011	0	0	0	0	0	0	0	0	0
010	1	0	0	0	0	0	0	0	0
100	0	0	0	0	0	0	0	0	0
101	0	0	0	0	0	0	0	0	0
111	0	0	0	0	0	0	1	0	0
110	0	0	0	0	0	0	1	0	0

 $\frac{1}{2}$ $\frac{1}{2}$

$$C+ = DC-$$

$$C+ = NA.NB.NC.ND.E.NF + NA.B.C.ND.NE.NF + A.B.C.ND.NE.NF + A.B.C.D.E.F + A.B.C.D.E.NF$$

 $\times$

$D+$

	ABC							
DEF	000	001	011	010	100	101	111	110
000	0	0	0	0	0	0	0	1
001	0	0	0	0	0	0	0	0
011	0	0	0	0	0	0	0	0
010	1	0	0	0	0	0	0	0
100	0	0	0	0	0	0	0	0
101	0	0	0	0	0	0	0	0
111	0	0	0	0	0	0	0	0
110	0	0	0	0	0	0	1	0

$$D+ = DD.$$

$$D+ = NA \cdot NB \cdot NC \cdot ND \cdot E \cdot NF + A \cdot B \cdot NC \cdot ND \cdot NE \cdot NF + A \cdot B \cdot C \cdot D \cdot E \cdot NF.$$

 $E+$ ABC

	ABC							
DEF	000	001	011	010	100	101	111	110
000	0	0	0	0	0	0	0	0
001	0	0	0	0	0	0	0	0
011	0	0	0	0	0	0	0	0
010	1	0	0	0	0	0	0	0
100	1	0	0	0	0	0	0	0
101	0	0	0	0	0	0	0	0
111	0	0	0	0	0	0	0	0
110	0	0	0	0	0	0	1	0

$$E+ = DE.$$

$$E+ = NA \cdot NB \cdot NC \cdot ND \cdot E \cdot NF + NA \cdot NB \cdot NC \cdot D \cdot NE \cdot NF + A \cdot B \cdot C \cdot D \cdot E \cdot NF.$$

 $F+$

	ABC							
DEF	000	001	011	010	100	101	111	110
000	0	0	0	0	0	0	0	0
001	0	0	0	0	0	0	0	0
011	0	0	0	0	0	0	0	0
010	0	0	0	0	0	0	0	0
100	0	0	0	0	0	0	0	0
101	0	0	0	0	0	0	0	0
111	0	0	0	0	0	0	0	0
110	0	0	0	0	0	0	1	0

$$F+ = DF.$$

$$F+ = A \cdot B \cdot C \cdot D \cdot E \cdot NF.$$

- (ii) The 6 bit register will run through a reduced number of test vectors at the sample rate of a clock. The inputs to the CUT will be determined by the individual logic gates. This will then drive a test sequence which will result in a no fault condition. If a fault was present then it would produce an error at the output node. The fault is then detected and can be made evident through the EX-OR gate which can be used as a comparator against the input logic functions to determine the fault.

Question 2.

(a)

$$(i) \quad STD = \frac{0.05}{2} \quad STD = 0.025. \checkmark 2$$

Upper spec	15.05	0.025	← sigma. σ
	15.025	0.025	
	14.975	0.025	mean 15mm
Lower spec.	14.95	0.025	✓ 4

(ii) 6 σ (sigma).

$$(ii) \quad Cp = \frac{\text{Upper specification} - \text{Lower specification}}{6\sigma}$$

$$Cp = \frac{15.05 - 14.95}{6 \times 0.025.}$$

$$Cp = 0.6. \checkmark 3$$

Not capable as below 1.
Not capable as < 1 .

Minimum = 3 σ (sigma).

$$STD = \frac{0.05}{3.} \quad STD = 0.016.$$

$$Cp = \frac{15.05 - 14.95}{6 \times 0.016.}$$

$$Cp = 1.04 \text{ (2.d.p.)}$$

Capable as above 1. ✓ 3
Capable as > 1 .

(ii) The process is not capable at 6 sigma as it is below 1, but it is capable at the minimum capability requirement of 3 sigma as the result was greater than 1. ✓ part of Q2 (ii)

(ii) In this case 6 sigma must fit between the upper and lower specifications ~~at~~ either side of the mean at least once to be capable. If not then it is not considered capable. ✓ 3

(b)

$$(i) \quad STD = \frac{0.05}{4.} \quad STD = 0.0125. \checkmark 1$$

Upper spec	15.05	0.0125	
	15.0375	0.0125	
	15.025	0.0125	
	15.0125	0.0125	
	14.9875	0.0125	mean 15mm
	14.975	0.0125	
	14.9625	0.0125	
Lower spec	14.95	0.0125	

upper specification limits: ✓ 1
15.0125, 15.025, 15.0375, 15.05

lower specification limits:
14.9875, 14.975, 14.9625, 14.95.

(b)

$$(ii) Cpk = \min \left(\frac{\text{mean} - \text{Lower spec}}{3\sigma}, \frac{\text{Upper spec} - \text{mean}}{3\sigma} \right)$$

$$\text{L spec. } \frac{15.02 - 14.95}{3 \times 0.0125} = 1.86$$

$$\text{U spec. } \frac{15.05 - 15.02}{3 \times 0.0125} = 0.8$$

$$Cpk \min 1.86, 0.8$$

Not capable as both must be above 1.

(iii) In this case the 4 Sigma is not capable as it must fit between the upper and lower specifications on either side of the mean at least once. Both sides of the mean must be greater than 1 if it is to be considered capable. This is not the case here. Both sides are not greater than 1. Only one side is greater than one, but both sides must be greater than 1 to be capable. Therefore, the 4 Sigma is not capable.

(vi) It does not.

Capability ratio is not suitable as it does not take into account discrepancies, for example wear and tear of machine parts into consideration. These discrepancies have not been taken into account into the formulas when determining whether suitable or not.

Question 5.

d)

(ii)

10	20	50
10	150	50
10	20	50

CPE

1	1	1
1	1	1
1	1	1

1/9

~~10+20~~

$$10 + 20 = 30 \quad 10 + 150 = 160 = \frac{190}{9} \approx 21.1$$

$$20 + 50 = 70 \quad 150 + 50 = 200 = \frac{270}{9} = 30$$

$$10 + 150 = 160 \quad 10 + 20 = 30 = \frac{190}{9} = 21.1$$

$$150 + 50 = 200 \quad 20 + 50 = 70 = \frac{270}{9} = 30$$

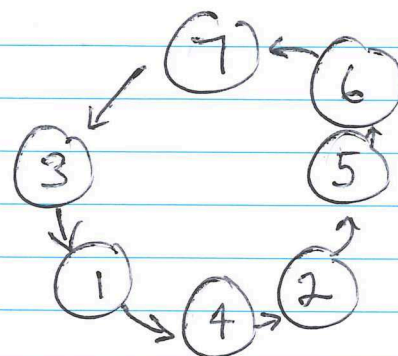
∴

21.1	30
21.1	30

Question 4.

(a)

(ii)



Anti clockwise
direction.
for the sequence.

4
3
1
6