

report

by Rhiannon Gallacher

FILE	3464_RHIANNON_GALLACHER_REPORT_158487_1472331216.DOCX		
TIME SUBMITTED	03-MAY-2018 04:44PM (UTC+0100)	WORD COUNT	3007
SUBMISSION ID	88266026	CHARACTER COUNT	22064

**BSc (Hons) Electrical & Electronic
Engineering**

Electronic Production & Test – PSDE 6018

Fault Modelling

TATA Steel

Rhiannon Gallacher

Contents

1.0 – Introduction.....	3
Table of Figures	4
2.0 - Research.....	5
2.1 – IC Fabrication Faults.....	5
2.2 - Single Stuck at Fault.....	5
2.3 - Electro Static Discharge	6
3.0 – Design of Assignment Requirements.....	10
4.0 – Analysis of NI MultiSim results	14
4.1 - Analysis of Tests Using Logic Analyser	14
4.2 - 6-Bit Register Test Design for ATE Alternative	17
5.0 – Practical build and test using LabVIEW.....	22
6.0 - Conclusion & Recommendations	26
7.0 - Bibliography	27

1.0 – Introduction

The aim of this assignment is to demonstrate knowledge of IC fabrication faults and the use of single stuck at fault modelling (SSF) and electro static discharge (ESD). This will be demonstrated by undertaking research into both areas and undertaking a practical experiment into SSF. The assignment should also demonstrate an understanding of the use of automatic test equipment (ATE) in testing IC and PCB systems.

The practical experiment will include designing and building a prototype of the combinational circuit shown in figure 3 on Multisim. Fault modelling techniques will be implemented using a stuck at fault table. The minimum number of test vectors must be produced. The circuit will then be built on the NI FPGA board and tested.

Table of Figures

Figure 1 - Electro Static – Safe Workbench	9
Figure 2 - Combinational Circuit.....	10
Figure 3 - NAND, NOR, AND and OR tables	10
Figure 4 – Multisim Test Circuit	12
Figure 5 - PWL Source Setup	12
Figure 6 – Multisim Circuit Results.....	13
Figure 7 - MultiSim Fault Table	14
Figure 8 - Multisim Fault One Circuit	14
Figure 9 - Multisim Fault One Results	14
Figure 10 - Multisim Fault Two Circuit	15
Figure 11 - Multisim Fault Two Results.....	15
Figure 12 - Multisim Fault Three Circuit	16
Figure 13 - Multisim Fault Three Results.....	16
Figure 14 - Multisim Circuit.....	20
Figure 15 - Multisim Results	21
Figure 16 - LabVIEW Circuit.....	22
Figure 20 – Test 3	23
Figure 19 – Test 2	23
Figure 18 – Test 1	23
Figure 17 – Test 0	23
Figure 24 - Test 7.....	23
Figure 23 – Test 6	23
Figure 22 – Test 5	23
Figure 21 - Test 4.....	23
Figure 25 - Fault One FPGA Board.....	24
Figure 26 - Fault One LabVIEW Screen	24
Figure 27 – Fault Two LabVIEW Screen	24
Figure 28 – Fault Two FPGA Board.....	24
Figure 30 – Fault Three FPGA Board.....	25
Figure 29 – Fault Three LabVIEW Screen.....	25

*This section should be before
the introduction.*

2.0 - Research

2.1 – IC Fabrication Faults

There are two groups of IC fabrication faults: logical faults and physical faults, logic faults are usually caused as a result of a physical fault.

An example of a logical fault would be, a degradation fault is a timing issue, and this type of fault may lead to an incorrect switching threshold in a TTL/CMOS level converter at an input. This fault can be tested using a production tester. A delay fault could lead to a path being slower than required by the specification.

An open circuit fault is a result of a physical fault, this may be due to a bad contact or over-etching. This type of fault would cause a failure to transmit a logic level.

A short circuit fault is a result of a physical fault such as under-etching or spiking. This causes sections of the circuit being connected when they shouldn't be. Bridging faults are similar however, more often caused by metal coverage problems leading to shorts.

2.2 - Single Stuck at Fault

A single stuck a fault is a type of fault modelling that can be used by fault simulators and automatic test pattern generation tools to mimic faults in an integrated circuit. Instead of testing all possible combinations of 0's and 1's a model can be used with a reduced set of vectors. The single stuck at fault model can be used to test each node of the circuit in turn. There are two faults; stuck at 0 (Short circuit to ground) and stuck at 1 (short circuit to supply rail). The number of faulty circuits requiring simulating is decided by $n + 1$, the n is decided by the number of circuit nodes. With a stuck at fault a pattern of 1's and 0's can be applied to the logic gate so you will get a faulty response. For example, with an inverter gate, if you suspect the input is stuck at 1, a 0 would be put on the input. It would then be expected that a 1 would be shown on the output. If a 0 is shown there is a stuck at fault. The full stuck at table can be seen in table 1.

Table 1 – Inverter gate Stuck at Fault Table

S@Fault	Test Input	Pass Output	Fail Output
Input S@1	0	1	0
Input S@0	1	0	1
Output S@1	1	0	1
Output S@0	0	1	0

Even though there are 4 tests shown in the table, there are only two different tests. Therefore, it would only take two tests to prove this gate, this is known as fault collapsing.

The same principle can be applied to NAND gates, table 2 shows the fault basis.

Table 2 - NAND Gate Stuck at Table

S @ Fault	Test Input A	Test Input B	Pass Output	Fail Output
A S@1	0	1	1	0
A S@0	1	1	0	1
B S@1	1	0	1	0
B S@0	1	1	0	1
Output S@1	1	1	0	1
Output S@0	1	0	1	0
Output S@0	0	1	1	0

This table is slightly more complex as it has two inputs and an output. However, it can be reduced to 3 tests. The tests required are;

Table 3 - Reduced NAND Table

A	B	S@Fault detected
1	0	OutputS@0, B S@1
1	1	A S@0, B S@0, Output S@1
0	1	A S@1, Y S@0

These tests can detect all six possible faults. However, it is only possible to detect one fault at a time. The above are just two examples of the single stuck at fault modelling. (Meixner, 2018)

2.3 - Electro Static Discharge

Bringing two materials together repeatedly produces static electricity through the triboelectric phenomenon. All materials are made up of atoms. Atoms have a positive core which is surrounded by electrons. When two materials make contact, if one material has atoms which attracts atoms more strongly than the other it is possible that when the materials are separated electrons can jump to the atom with the greater attraction. The atom that gains electrons becomes negatively charged and the one that loses the electrons becomes positively charged. The longer that materials are exposed to one another the more electrons can jump across. This is how static charge builds up. Depending on the material, some will gain positive charge and others will gain negative charge. The amount of charge gained also varies between materials.

Generally, it can be said that minerals gain positive charge, wood and paper have neutral charge and plastics and metals gain negative charge. Many websites and books list what is known as the triboelectric series, this lists materials in order of the charge they gain from positive to negative. The further away from each other two materials are on this list the greater the static charge that will build between them, the closer the two materials the harder it would be to build static charge between them. (Woodford, 2018)

Electro static discharge is the release of static electricity. This occurs when two objects come into contact and have different levels of electro static charge. ESD can often be felt when an individual walks across a carpet and then proceeds to touch a metal doorknob. A higher level of ESD is lightning. Generally, ESD is harmless, however it can be a problem in industrial environments. The heat from the ESD is very hot although generally not felt. However, if the charge were to be released onto an electronic device, the heat would be enough to melt or vaporize the small parts of the board causing failure.

(Rouse, 1999-2018)

There are two categories that damage from ESD can be put into;

- Catastrophic damage – This would mean the electronic device became immediately inoperable after the ESD event. A semiconductor junction could have been damaged by the ESD.
- Latent damage – The electronic device will appear to function correctly after the ESD event however the sensitive circuitry has been damaged and may fail to operate correctly in the future. (Mini-Circuits, 2015)

Catastrophic damage is less costly in the manufacturing stage as it can be detected and resolved early on. Latent damage is potentially more costly as it may not be detected in the normal inspection process and the product may be completed and shipped out to the customer without the damage being detected.

Static charge is generated from many everyday activities, the level of charge generated can vary. This can be seen in figure 1. Humans will not actually feel the ESD unless it is over 3000 volts. (CISCO, 2018)

Walking across a carpet	1,500-35,000 volts
Crossing your legs	300 volts
Walking over an untreated vinyl floor	250-12,000 volts
Working at a bench	700-6,000 volts
Vinyl envelope for work instructions	600-7,000 volts
Picking up common plastic bag from bench	1,200-20,000 volts
Work chair padded with polyurethane foam	1,500-18,000 volts
Touching a door knob or metal object	1,500-35,000 volts
Standing up from a chair	hundreds of volts

Figure 1 - Causes of Static Charge

Although humans can withstand this, many components cannot. The typical voltage that will damage electronic devices are as follows:

- MOSFET – 100 to 200 Volts
- JFET – 140 to 10,000 Volts
- CMOS – 250 to 2,000 Volts
- Schottky diodes – 300 to 10,000 Volts
- Bi-polar transistors - 380 to 10,000 Volts
- SCR – 680 to 1000 Volts

(Electronic Imaging Materials, 2018)

There are methods that can be used to protect electronic devices from ESD. For example, items can be bought to reduce the likelihood of ESD such as wrist straps, shoe sole grounder and conductive shoes. Other steps that can be taken to reduce the chance of causing ESD are,

- Check humidity, having a humidity level of 40 to 90% reduces the resistance of items that may generate a charge, this make it more difficult for the items to generate ESD
- Provide common ground for all ESD components. This ensures any built up ground can be safely discharged.
- Keep all components in anti-static bags until needed. These bags prevent charge from building
- Ensure personal static charge has been discharged before starting work on electronic components

(Micro Electronics Inc, 2018)

Figure 2 shows a static-safe workbench. This includes a static dissipative mat which is grounded through a 1 Meg-ohm resistor, which covers the bench. The resistor protects the user in the event that the bench should become live. Figure 2 also shows a wrist strap being worn and anti-static materials and tools being used. Antistatic floor tiles and an antistatic smock worn by the workers further enhance the static safe work environment.

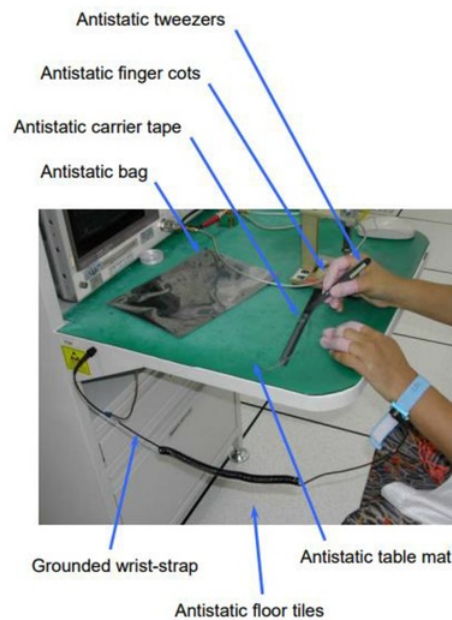


Figure 2 - Electro Static – Safe Workbench

Overall the research is good with a wide range of examples. The sources are limited and the IC fabrication faults could improve.

3.0 – Design of Assignment Requirements

The combinational circuit that will be modelled can be seen in figure 3.

4 shows the gate tables for each component. The truth tables have been reduced down to the minimum variances to test the entire component with the minimum test vectors. These gate tables are then combined into a derived table to test the whole circuit; shown in **Error!**
Reference source not found..

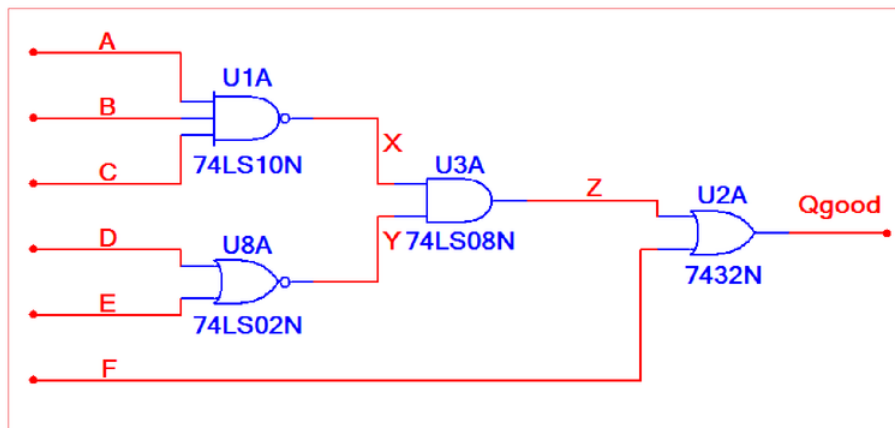


Figure 3 - Combinational Circuit

NAND

A	B	C	X
1	1	1	0
0	1	1	1
1	0	1	1
1	1	0	1

NOR

D	E	Y
0	0	1
1	0	0
0	1	0

AND

X	Y	Z
1	1	1
0	1	0
1	0	0

OR

Z	F	QGOOD
0	0	0
0	1	1
1	0	1

Figure 4 - NAND, NOR, AND and OR tables

Good examples of fault models.
There should be a heading to
identify these as fault models
which can be used for the test
circuit.

Table 4 - Derived Table

Test No	NAND Gate			NOR Gate		OR		Q good	HEX	AND Gate		OR	Fault
	A	B	C	D	E	F				X	Y	Z	
1	1	1	1	0	0	0	0	0	70	0	1	0	A+B+C SA0X
2	0	1	1	0	0	0	1	1	31	1	1	1	A SA1
3	1	0	1	0	0	0	1	1	51	1	1	1	B SA1
4	1	1	0	0	0	0	1	1	61	1	1	1	C SA1
5	0*	0*	0*	0	0	0	1	1	1	1	1	1	D+E SA1 X+Y SA0,
6	0*	0*	0*	1	0	0	0	0	8	1	0	0	D SA0
7	0*	0*	0*	0	1	0	0	0	4	1	0	0	E SA0
8	0*	0*	0*	0	0	0	1	1	1	1	1	1	X+Y SA0
9	1	1	1	0	0	0	0	0	70	0	1	0	X SA1
10	0*	0*	0*	1**	1** 0	0	0	0	0C	1	0	0	Y SA1
11	1	1	1	1**	1**	0	0	0	7C	0*	0*	0	F+Z SA1
12	1	1	1	1**	1**	1	1	1	7F	0*	0*	0	F SA0
13	0*	0*	0*	0	0	0	0	1	1	1	1	1	Z SA0

* Indicates all or at least 1 must be at logic 0 for correct results

**Indicates all or at least 1 must be at logic 1 for correct result

Table 4 shows the test vectors obtained from the gate tables in figure 4. The input variables are shown in red. The expected output can be seen in blue. The HEX values are a quick and easy way of seeing which lines are repeats. Repeated tests can be eliminated from the table.

Table 5 - Reduced table

Test No	NAND Gate			NOR Gate		OR		Q good	HEX	AND Gate		OR	Fault
	A	B	C	D	E	F				X	Y	Z	
1	1	1	1	0	0	0	0	0	70	0	1	0	A+B+C SA0X SA1
2	0	1	1	0	0	0	1	1	31	1	1	1	A SA1
3	1	0	1	0	0	0	1	1	51	1	1	1	B SA1
4	1	1	0	0	0	0	1	1	61	1	1	1	C SA1
5	0*	0*	0*	0	0	0	1	1	1	1	1	1	D+E SA1 X+Y SA0,
6	0*	0*	0*	1	0	0	0	0	8	1	0	0	D SA0
7	0*	0*	0*	0	1	0	0	0	4	1	0	0	E SA0
8	0*	0*	0*	1**	1** 0	0	0	0	0C	1	0	0	Y SA1
9	1	1	1	1**	1**	0	0	0	7C	0*	0*	0	F+Z SA1
10	1	1	1	1**	1**	1	1	1	7F	0*	0*	0	F SA0

* Indicates all or at least 1 must be at logic 0 for correct results

**Indicates all or at least 1 must be at logic 1 for correct result

Table 5 shows the table obtained once the repeated lines had been removed. Variables marked by * or ** are conditional don't care states. These can be altered to match a different line and make the Hex value match, as long as the actual output isn't changed. Test 5 was eliminated by altering A and B to 1. This makes it a repeat of test 4. Test 10 can be eliminated by altering E to 0, making it a repeat of test 6.

Table 6 - Final Table

Test No	NAND Gate			NOR Gate			OR	Q good	HEX	AND Gate			Fault
	A	B	C	D	E	F				X	Y	Z	
1	1	1	1	0	0	0	0	0	70	0	1	0	A+B+C SA0X SA1
2	0	1	1	0	0	0	1	1	31	1	1	1	A SA1
3	1	0	1	0	0	0	1	1	51	1	1	1	B SA1
4	1	1	0	0	0	0	1	1	61	1	1	1	C SA1
6	0*	0*	0*	1	0	0	0	0	8	1	0	0	D SA0
7	0*	0*	0*	0	1	0	0	0	4	1	0	0	E SA0
9	1	1	1	1**	1**	0	0	0	7C	0*	0*	0	F+Z SA1
10	1	1	1	1**	1**	1	1	1	7F	0*	0*	0	F SA0

Table 6 shows the final table with the minimum possible number of tests required to prove the entire circuit.

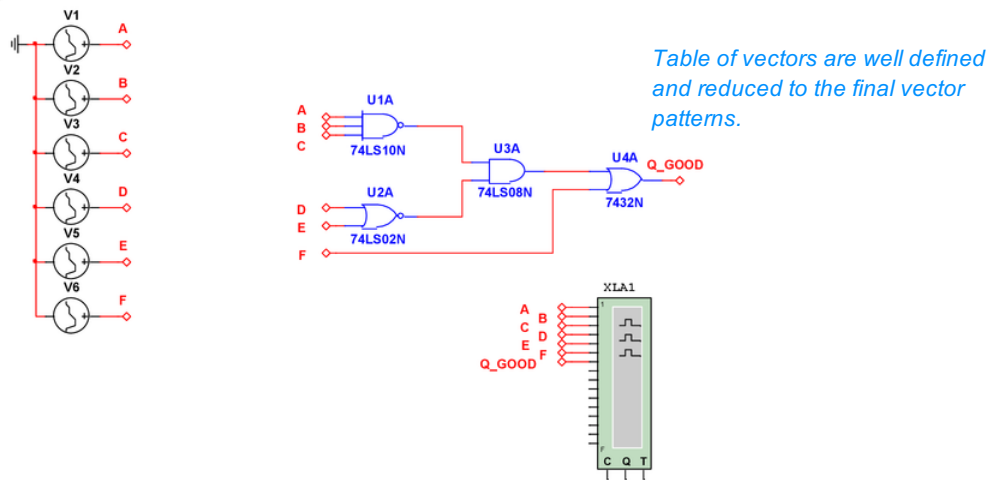


Figure 5 – Multisim Test Circuit

The circuit was built in Multisim to test the circuit. This can be seen in figure 5. To alter the voltage to each input pulse width length sources have been used. Figure 6 shows the timings of the PWL sources.

Label

Display

Value

Fault

Pins

Variant

User fields

☐ Use data directly from file

File name:

Browse...

Edit file

☒ Enter data points in table

Time

Voltage

0ms	5
9.99ms	5
10ms	0
19.99ms	0
20ms	5
39.99ms	5
40ms	0
59.99ms	0
60ms	5

Figure 6 - PWL Source Setup

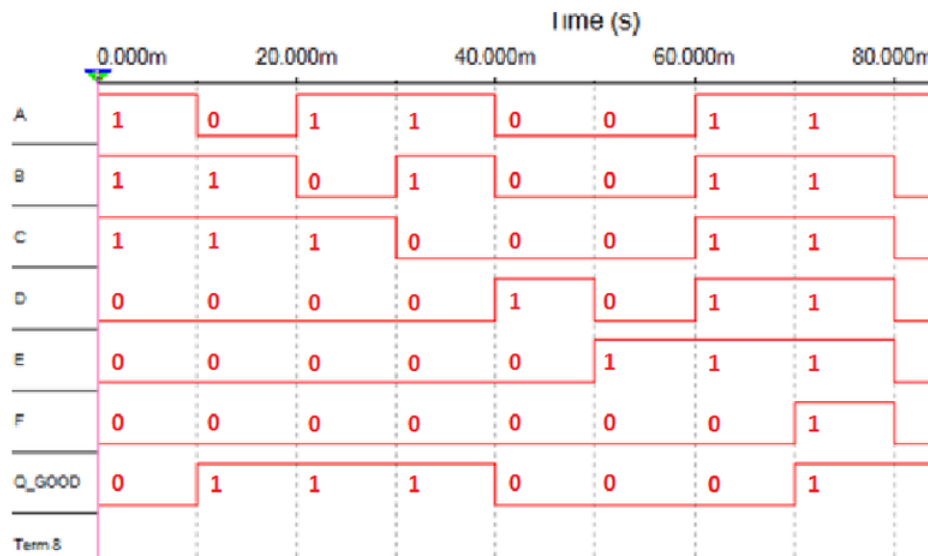


Figure 7 – Multisim Circuit Results

The results from the testing can be seen in figure 7. Comparing the results to those shown in table 6 it can be seen that the circuit worked as expected.

There should be a reference to the X-O

4.0 – Analysis of NI MultiSim results

4.1 - Analysis of Tests Using Logic Analyser

Table 8 shows three of the tests with faults placed in them. The faults were used to test the operation of the circuit.

Test No	A	B	C	D	E	F	Q good	HEX	X	Y	Z	Fault
1	0	1	1	0	0	0	0	70	0	1	0	A+B+C SA0X
7	0*	0*	0*	0	0	0	0	4	1	0	0	E SA0
10	1	1	1	1**	1**	0	1	7F	0*	0*	0	F SA0

Figure 8 - MultiSim Fault Table

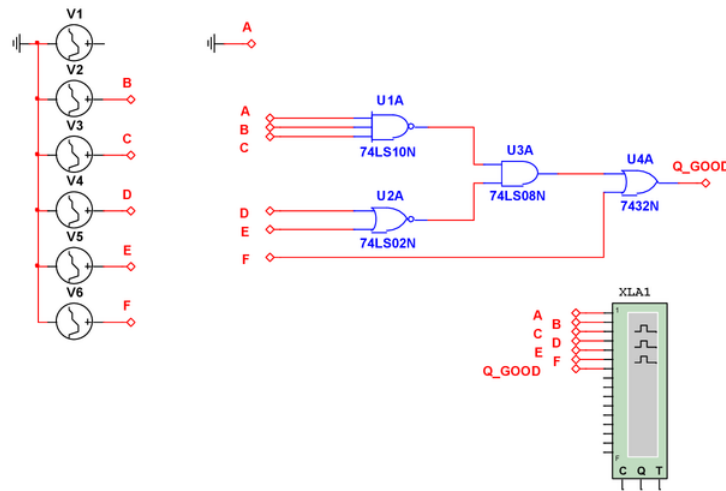


Figure 9 - Multisim Fault One Circuit

Figure 9 shows that the first fault has been placed on the circuit by holding A down to zero.

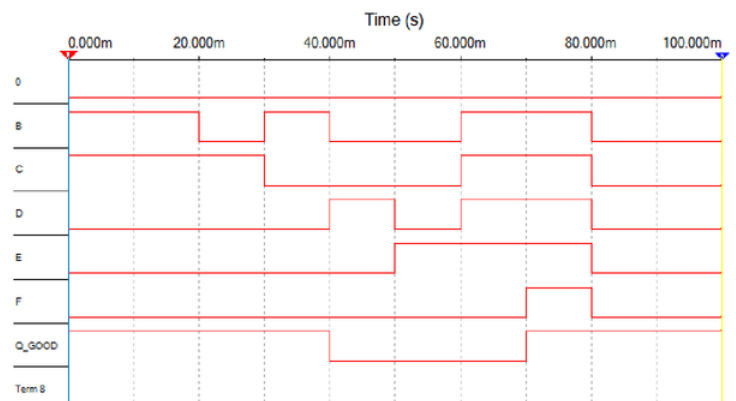


Figure 10 - Multisim Fault One Results

Figure 10 shows the results obtained from Multisim after the first fault was placed on the circuit. With A being held down to zero it can be seen that for the first 10mS of the graph Q_GOOD is high as opposed to figure 7 where Q_GOOD was low.

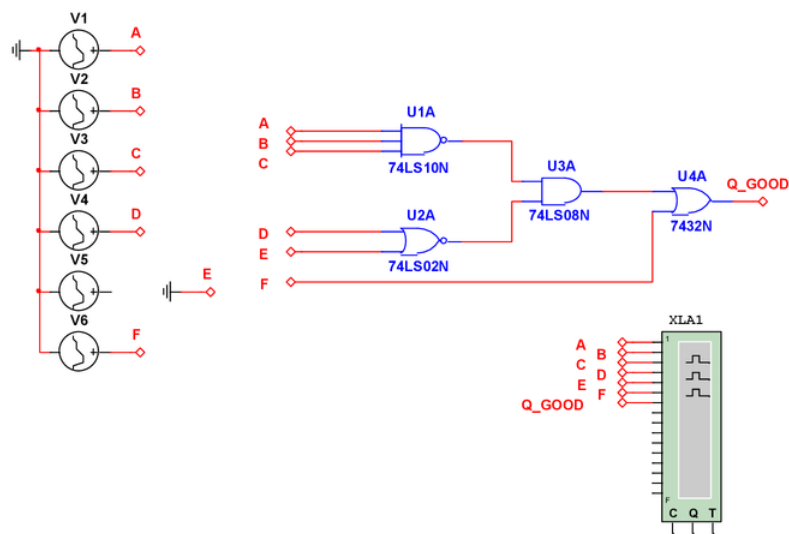


Figure 11 - Multisim Fault Two Circuit

Figure 11 shows that input E is now being held down to zero. From the results shown in figure 12 it can be seen that this causes Q_GOOD to become high between 50 and 60 mS.

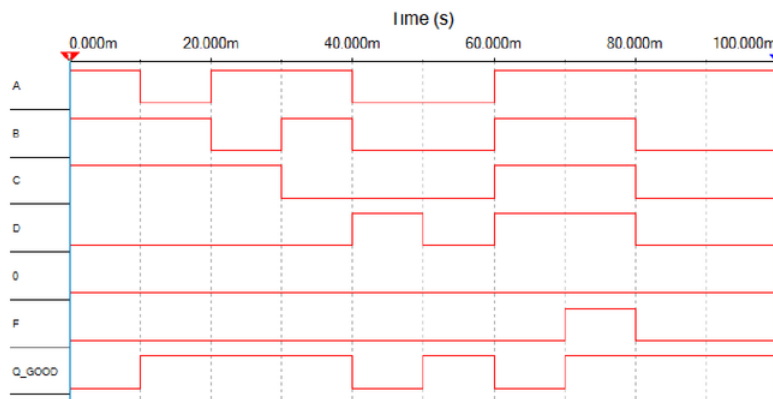


Figure 12 - Multisim Fault Two Results

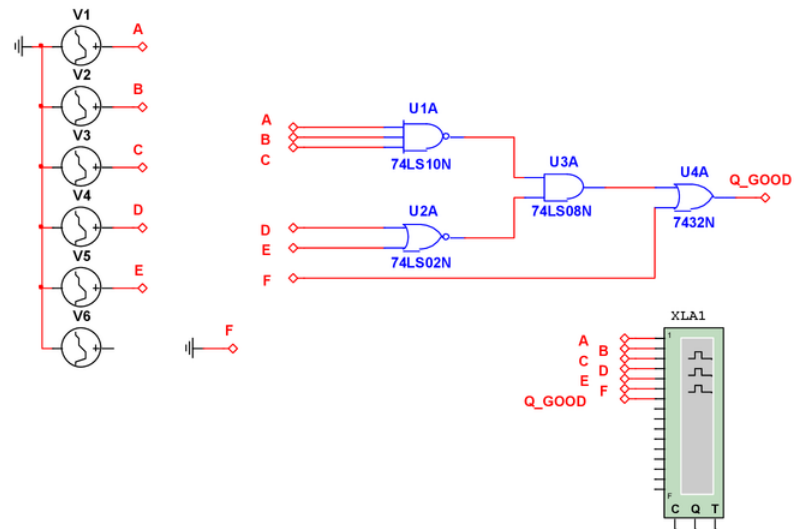


Figure 13 - Multisim Fault Tree Circuit

Figure 13 shows that input F has been held down to zero. Figure 14 shows that this causes Q_GOOD to go high at 80mS as opposed to 70mS.

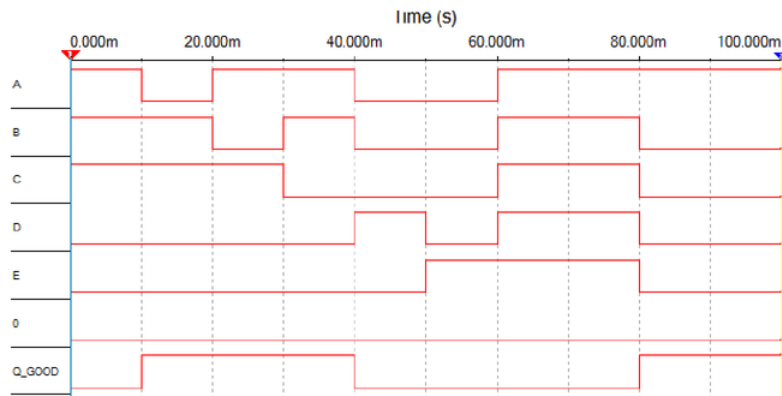


Figure 14 - Multisim Fault Tree Results

*Test faults are shown
but they should be
demonstrated using a
X-OR gate
comparator.*

4.2 - 6-Bit Register Test Design for ATE Alternative

Table 7 shows the circuit's truth table. This table was used to generate Karnaugh maps for individual circuits which can then be used to generate signals for each input.

Present State						Next State					
A	B	C	D	E	F	A+	B+	C+	D+	E+	F+
1	1	1	0	0	0	0	1	1	0	0	0
0	1	1	0	0	0	1	0	1	0	0	0
1	0	1	0	0	0	1	1	0	0	0	0
1	1	0	0	0	0	0	0	0	1	0	0
0	0	0	1	0	0	0	0	0	0	1	0
0	0	0	0	1	0	1	1	1	1	1	0
1	1	1	1	1	0	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	0	0	0

Table 7 - Circuit Truth Tables

Table 10 shows the Karnaugh map for input A. The red indicates the groups which were used to produce the Boolean expression. This process was repeated for all inputs

Table 9 - Input A Karnaugh Map

A+		ABC							
DEF	ABC	000	001	011	010	100	101	111	110
000	000	0	0	1	0	0	1	0	0
001	001	0	0	0	0	0	0	0	0
011	011	0	0	0	0	0	0	0	0
010	010	1	0	0	0	0	0	0	0
100	100	0	0	0	0	0	0	0	0
101	101	0	0	0	0	0	0	0	0
111	111	0	0	0	0	0	0	1	0
110	110	0	0	0	0	0	0	1	0

$$N = A.B.C.D.E + A.NB.C.ND.NE.NF + NA.B.C.ND.NE.NF + NA.NB.NC.ND.E.NF$$

Table 8 - Input B Karnaugh Map

B+		ABC							
DEF	ABC	000	001	011	010	100	101	111	110
000	000	0	0	0	0	0	1	1	0
001	001	0	0	0	0	0	0	0	0
011	011	0	0	0	0	0	0	0	0
010	010	1	0	0	0	0	0	0	0
100	100	0	0	0	0	0	0	0	0
101	101	0	0	0	0	0	0	0	0
111	111	0	0	0	0	0	0	1	0
110	110	0	0	0	0	0	0	1	0

$$N = A.C.ND.NE.NF + A.B.C.D.E + NA.NB.NC.ND.E.NF$$

C+ Table 12 - Input C Karnaugh Map

ABC									
DEF		000	001	011	010	100	101	111	110
	000	0	0	1	0	0	0	1	0
	001	0	0	0	0	0	0	0	0
	011	0	0	0	0	0	0	0	0
	010	1	0	0	0	0	0	0	0
	100	0	0	0	0	0	0	0	0
	101	0	0	0	0	0	0	0	0
	111	0	0	0	0	0	0	1	0
	110	0	0	0	0	0	0	1	0

$$N = B.C.ND.NE.NF + A.B.C.D.E + NA.NB.NC.ND.E.NF$$

Table 11 - Input D Karnaugh Map

ABC									
DEF		000	001	011	010	100	101	111	110
	000	0	0	0	0	0	0	0	1
	001	0	0	0	0	0	0	0	0
	011	0	0	0	0	0	0	0	0
	010	1	0	0	0	0	0	0	0
	100	0	0	0	0	0	0	0	0
	101	0	0	0	0	0	0	0	0
	111	0	0	0	0	0	0	0	0
	110	0	0	0	0	0	0	1	0

$$N = NA.NB.NC.ND.E.F + A.B.NC.ND.NE.NF + A.B.C.D.E.NF$$

E+ Table 10 - Input E Karnaugh Map

ABC									
DEF		000	001	011	010	100	101	111	110
	000	0	0	0	0	0	0	0	0
	001	0	0	0	0	0	0	0	0
	011	0	0	0	0	0	0	0	0
	010	1	0	0	0	0	0	0	0
	100	1	0	0	0	0	0	0	0
	101	0	0	0	0	0	0	0	0
	111	0	0	0	0	0	0	0	0
	110	0	0	0	0	0	0	1	0

$$N = NA.NB.NC.ND.E.NF + NA.NB.NC.D.NE.NF + A.B.C.D.E.NF$$

Table 13 - Input F Karnaugh Map

F+									
DEF	ABC	000	001	011	010	100	101	111	110
	000	0	0	0	0	0	0	0	0
	001	0	0	0	0	0	0	0	0
	011	0	0	0	0	0	0	0	0
	010	0	0	0	0	0	0	0	0
	100	0	0	0	0	0	0	0	0
	101	0	0	0	0	0	0	0	0
	111	0	0	0	0	0	0	0	0
	110	0	0	0	0	0	0	1	0

$$N = A.B.C.D.E.NF$$

The circuit built in Multisim can be seen in figure 15. The main body of the circuit is built from D-type flip flops. As some expressions from the Karnaugh maps were the same the circuit was able to be compressed to three expressions labelled as Z1, Z2 and Z3.

The results obtained from Multisim can be seen in figure 16. The results show that the results can also be achieved using this alternative method.

*Good demonstration
of 6 variable k-map
design for circuit
reduction and use of
the mirror method*

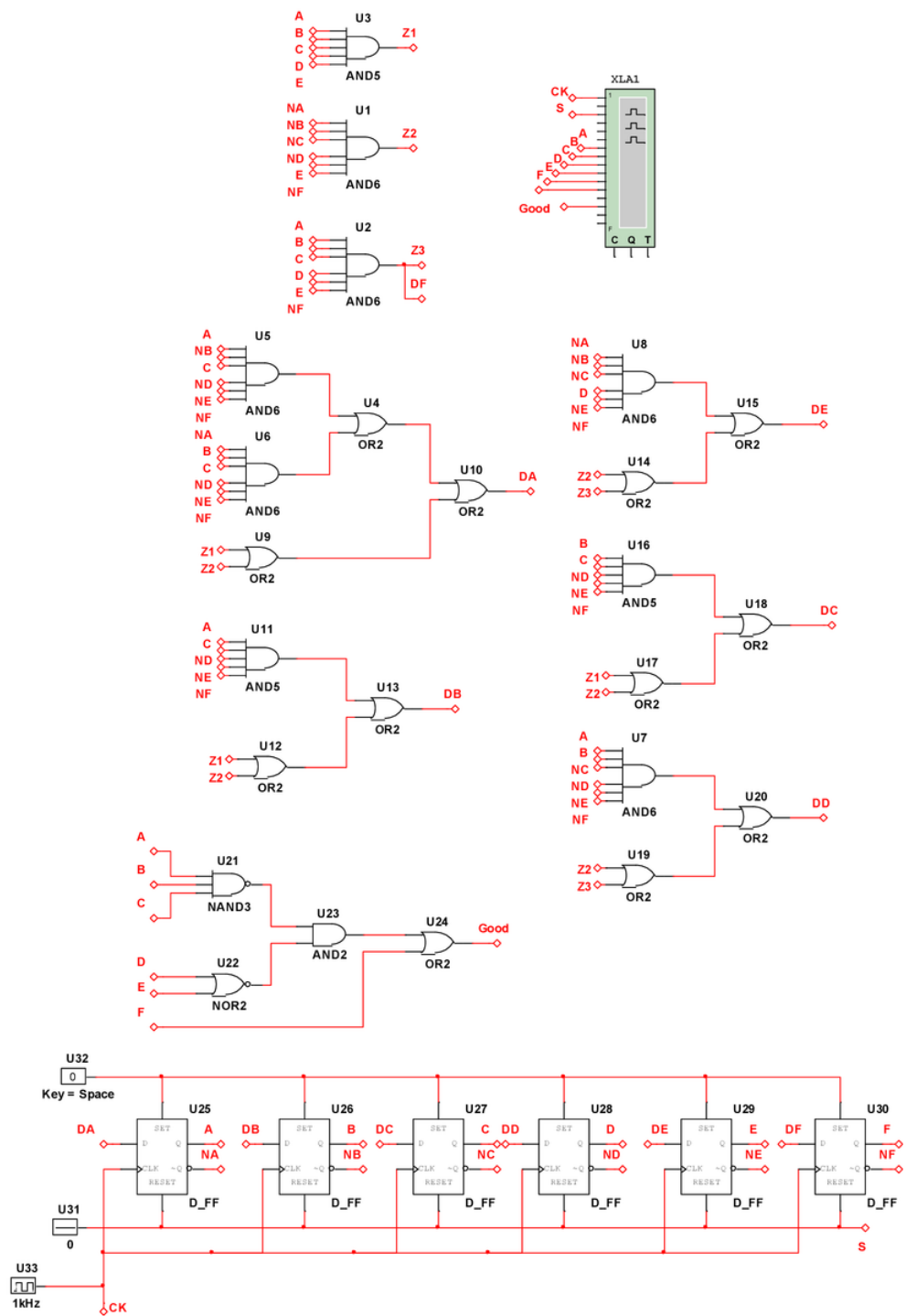


Figure 15 - Multisim Circuit

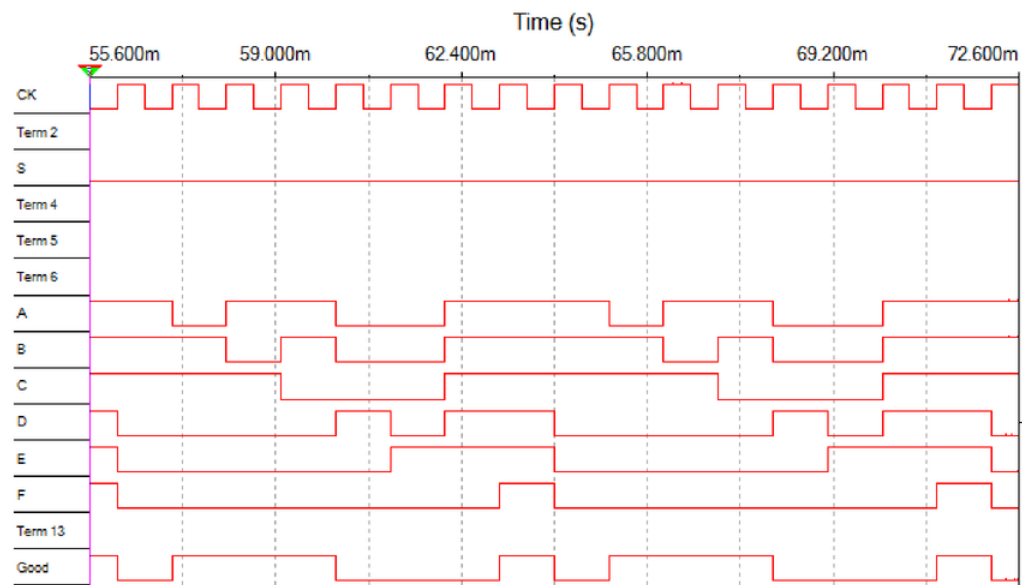


Figure 16 - Multisim Results

This is correct and shows the correct test vectors for the test circuit inputs. This should have included the X-OR gate and the cursors should have been used to define the start and end of test vectors.

5.0 – Practical build and test using LabVIEW

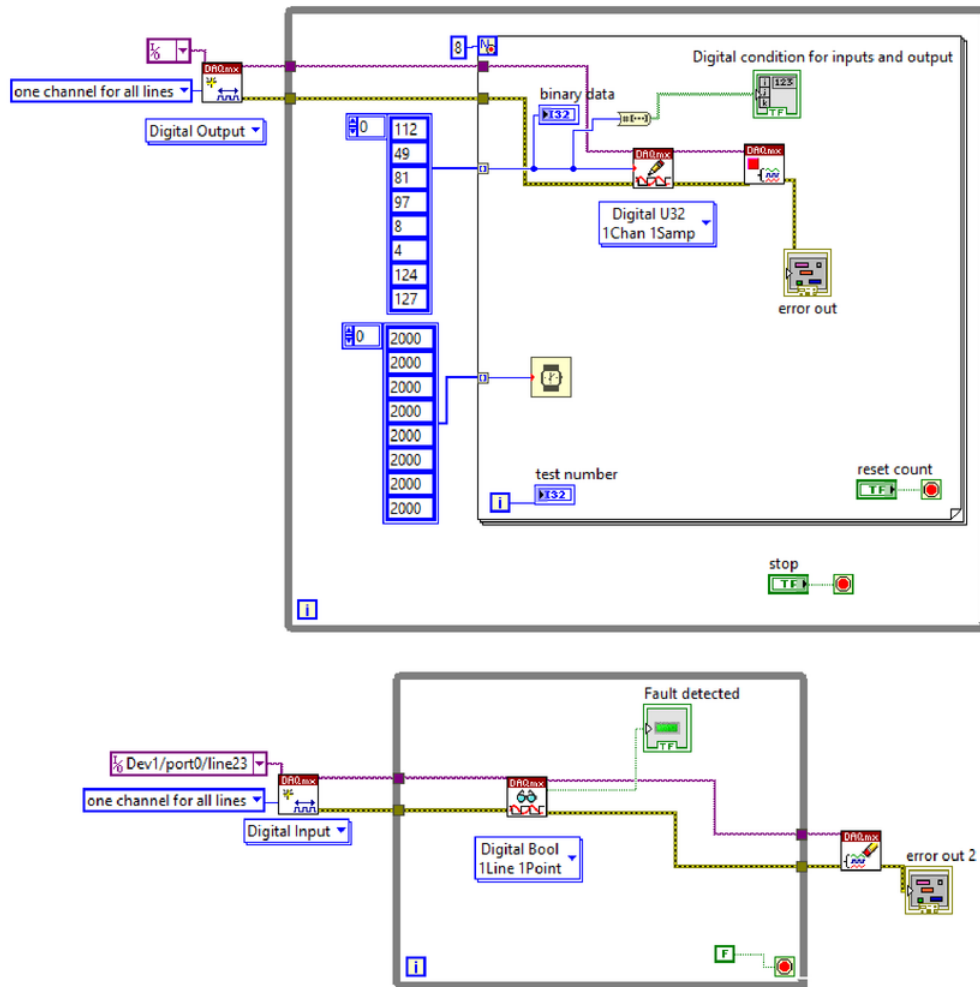


Figure 17 - LabVIEW Circuit

A LabVIEW circuit was designed and built to enable the IC to be tested. This can be seen in figure 17 Inside the while loop is a for loop. The blue arrays house the decimal values which control the inputs. The condition of the inputs and outputs can be seen by using the digital condition box. There are 8 steps in the for loop, each step lasts a programmed 2 seconds, In each step the required decimal value is looked at and is outputted to the digital output task. This decimal value is then compared to the IC value. If there is a fault in the IC there will be a

difference in the XOR signal and an output will be present. This will then energise the fault light.

Figures 18 through 23 show the process working through with no errors. The digital condition LED indicators show the state of the inputs and outputs. The binary data is the value to the IC.

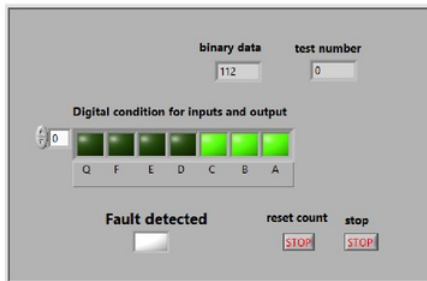


Figure 21 – Test 0

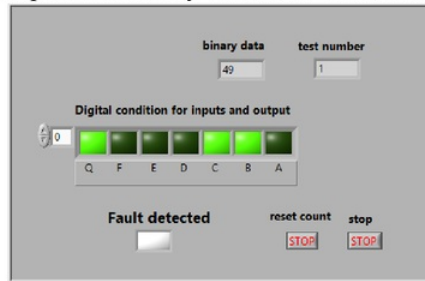


Figure 18 – Test 1

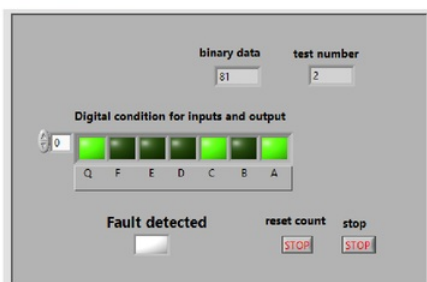


Figure 20 – Test 2

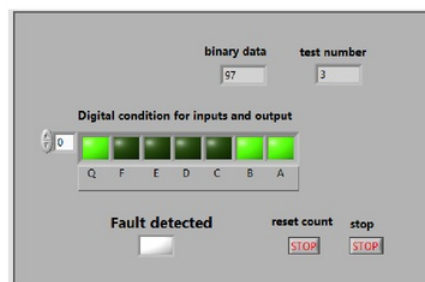


Figure 19 – Test 3

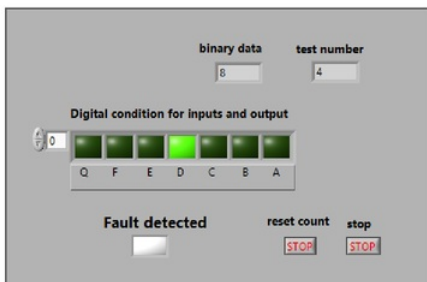


Figure 25 - Test 4

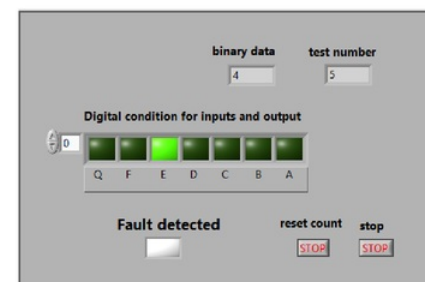


Figure 24 – Test 5

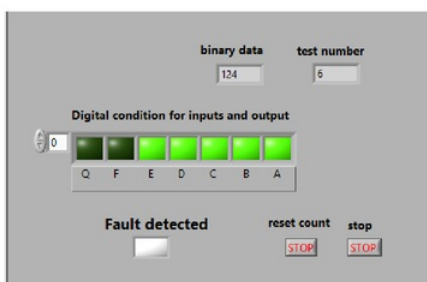


Figure 23 – Test 6

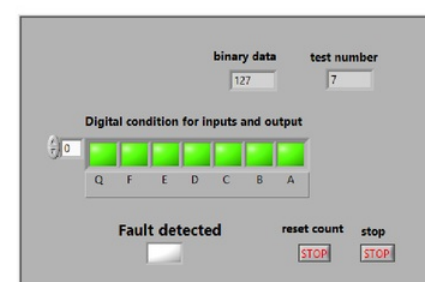


Figure 22 - Test 7

Faults were put on the circuit to demonstrate operation.

FAULT 1: INPUT A SA0

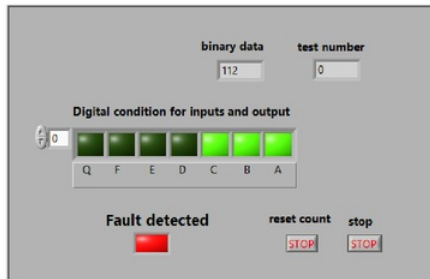


Figure 27 - Fault One LabVIEW Screen

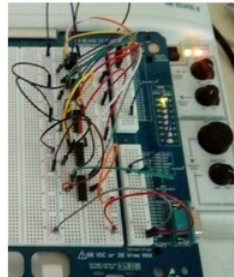


Figure 26 - Fault One FPGA Board

Figure 27 shows the first fault placed on the circuit. Input A connected to 0V. The LabVIEW front panel shows that Input A should be on, however the difference caused a change in the logic meaning XOR gate has activated and the fault LED shown.

FAULT 2: INPUT D SA0

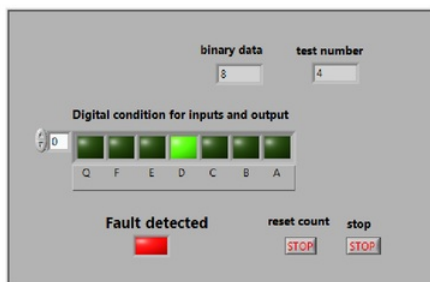


Figure 28 - Fault Two LabVIEW Screen

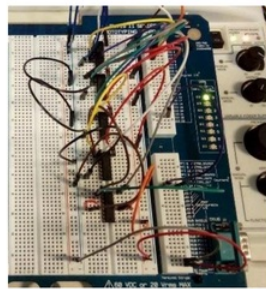


Figure 29 - Fault Two FPGA Board

Figure 28 shows the second fault placed on the circuit. Input D was connected to 0V. The LabVIEW front panel shows that input D should be on, however the difference caused a change in the logic meaning XOR gate has activated and the fault LED shown.

FAULT 3: INPUT F SA0

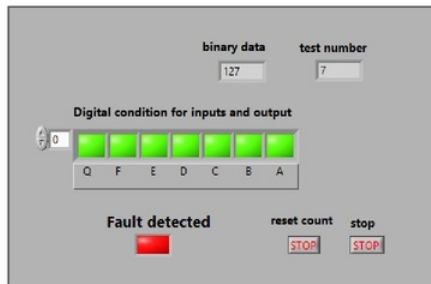


Figure 31 – Fault Three LabVIEW Screen

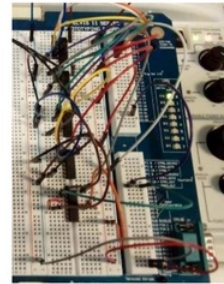


Figure 30 – Fault Three FPGA Board

Figure 31 shows the third fault placed on the circuit. Input F was connected to 0V. The LabVIEW front panel shows that input F should be on, however the difference caused a change in the logic meaning XOR gate has activated and the fault LED shown.

This is good work and clearly shows your understanding of the LabVIEW DAQMX design process

6.0 - Conclusion & Recommendations

Research was undertaken into faults on IC's, single stuck at faults and ESD. Specifically, looking into what ESD is, how it is built up, the dangers of it and the methods of preventing it. The combinational logic circuit given in the assignment brief was modelled. Truth Tables were created and reduced. Testing tables were created and reduced to the smallest possible number. These were then used to test the built Multisim circuit. It was also proven that that there were multiple ways of achieving the desired circuit. The circuit was tested practically by using a LabVIEW program and NI Elvis board. Faults were placed on the circuit and the circuit worked as expected.

In conclusion, all aims and objectives were met, research was completed, and all circuits were designed, built, tested and operated as expected.

*This could be
more in depth
and pointed out
the best
methods for
testing the
circuit.*

7.0 - Bibliography

CISCO, 2018. *ESD Training program*, s.l.: CISCO.

Electronic Imaging Materials, 2018. *Electrostatic Discharge (ESD)*. [Online]
Available at: <https://barcode-labels.com/getting-started/labels/esd-article/>
[Accessed 3 April 2018].

Meixner, A., 2018. *Digital Circuits and the Stuck at Fault Model*. [Online]
Available at: <https://accendoreliability.com/digital-circuits-stuck-fault-model/>
[Accessed 17 April 2018].

Micro Electronics Inc, 2018. *How to : Prevent ESD*. [Online]
Available at: http://www.microcenter.com/tech_center/article/4671/how_to_prevent_esd
[Accessed 3 April 2018].

Mini-Circuits, 2015. *The Prevention and Control of Electrostatic Discharge (ESD) (AN-40-005)*, s.l.: Mini-Circuits.

Rouse, M., 1999-2018. *Electrostatic Discharge*. [Online]
Available at: <https://whatis.techtarget.com/definition/electrostatic-discharge-ESD>
[Accessed 3 April 2018].

Woodford, C., 2018. *Static Electricity*. [Online]
Available at: <http://www.explainthatstuff.com/how-static-electricity-works.html>
[Accessed 7 April 2018].

*Good sources but could
have been two or three
more relevant sources*

report

GRADEMARK REPORT

FINAL GRADE

GENERAL COMMENTS

Instructor

63/100

PAGE 1

PAGE 2

PAGE 3

PAGE 4

Text Comment. This section should be before the introduction.

PAGE 5

PAGE 6

PAGE 7

PAGE 8

PAGE 9

Text Comment. Overall the research is good with a wide range of examples. The sources are limited and the IC fabrication faults could improve.

PAGE 10

Text Comment. Good examples of fault models. There should be a heading to identify these as fault models which can be used for the test circuit.

PAGE 11

PAGE 12

Text Comment. Table of vectors are well defined and reduced to the final vector patterns.

PAGE 13

Text Comment. There should be a reference to the X-OR gate as the comparator here.

PAGE 14

PAGE 15

PAGE 16

Text Comment. Test faults are shown but they should be demonstrated using a X-OR gate comparator.

PAGE 17

PAGE 18

PAGE 19

Text Comment. Good demonstration of 6 variable k-map design for circuit reduction and use of the mirror method

PAGE 20

PAGE 21

Text Comment. This is correct and shows the correct test vectors for the test circuit inputs. This should have included the X-OR gate and the cursors should have been used to define the start and end of test vectors.

PAGE 22

PAGE 23

PAGE 24

PAGE 25

Text Comment. This is good work and clearly shows your understanding of the LabVIEW DAQMX design process

PAGE 26

Text Comment. This could be more in depth and pointed out the best methods for testing the circuit.

PAGE 27

Text Comment. Good sources but could have been two or three more relevant sources

GRADING FORM: CSG-RUBIC

RESEARCH-INFORMED LITERATURE



Research is good and using a wide range of examples. There are limited sources used. IC fabricated faults - 2.5/5 ESD - 3.5/5 SAF - 3/5

9/15

KNOWLEDGE AND UNDERSTANDING



Minimum test vectors have been derived for the design. There are some explanations missing as far as the X-OR gate comparator is concerned. - 6/10 LabVIEW test vector design is good and explained well. - 7/10 Multisim design is good and works ok, but is not complete without the X-OR comparator and its purpose. The PLD design alternative should be explained and then further comparison in the conclusion. - 6/10

19/30

ANALYSIS



CAD test results show the test work and prove the CUT integrity, but the X-OR gate should be included.- 6/10 Comparison to theory is demonstrated through design and test. - 3/5

9/15

PRACTICAL APPLICATION AND DEP.



Prototyping of CUT is demonstrated and proven. The X-OR gate should be included.- 6/10 LabVIEW

17/25

design and implementation and explanation is good -
11/15

SKILLS FOR PROFESSIONAL PRAC.



Deployment of software is good - 3.5/5 Report is
good despite some headings missing - 3.5/5
Conclusion - this is a little too brief and should
include more comparison of the testing covered.-
2/5

9/15