

Examination Answer Books

12 Pages

Instructions to Candidates

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SURNAME: ZAHADYAKTA

FORENAME(S): FARSHID

1	Student Number	1303044/1
2	Title of Examination Paper	Electronic Production and test
3	Module Code	PSDE 6018
4	Date and Time of Examination	10/05/2018 9:30 am
5	Examination Venue	C54
6	Seat Number	
7	Number of Answer Books handed in	

List the numbers of the questions you have attempted	Office Use
Q3	25
Q2	32
Q1	18
Office Use	73

a)

Single stuck at fault modelling is used because of its simplicity. If all single faults are detected then a high percentage of ^{multiple} faults can be detected.

The single stuck at model applies to every node of the circuit in turn. Faults are usually SA0 (shorted to ground) SA1 (shorted to supply). The model $n-1$ is used to

detect total number of faults, where n is the number of inputs. If multiple number of single stuck at ~~are~~

model is used then each input could have to any one of

the states which are good SA0, SA1. Total number of inputs

to be simulated is $n^3 - 1$, this may be impractical in large

circuits due to the number of faults. The use of fault

modelling can simplify the number of testing needed to be

done in a circuit.

3 ✓

Adar

Q3

b)

Step 1:- Insert fault ^{model} to reduce test on individual gates

using formula $m+1$ where m is the number of inputs.
Identify fault that each test locates.

Step 2:- Set the circuit so that the gate under testing:

output equals to output (0 good), i.e. if AND or NAND

gates are to be tested then all inputs must be set to

1 except the one that carries the fault.

for OR & NOR set to 0

Step 3:- Find redundant test vector using HEX value.

Step 4:- Take out values that are equal using HEX

mapping. No repetitions.

Step 5:- Use manipulation process to alter

conditions to further reduce the number of test vectors.

K-map for A^+

ABC

DEF	000	001	011	010	100	101	110
000	1						
001							
011							
010							
100							
101							
111							
110							

$$A^+ = DA = NA \cdot NB \cdot NC \cdot ND \cdot NE \cdot NF +$$

$$A \cdot B \cdot C \cdot ND \cdot NE +$$

$$A \cdot NB \cdot C \cdot ND \cdot E \cdot NF +$$

$$NA \cdot B \cdot C \cdot D \cdot NE \cdot NF$$

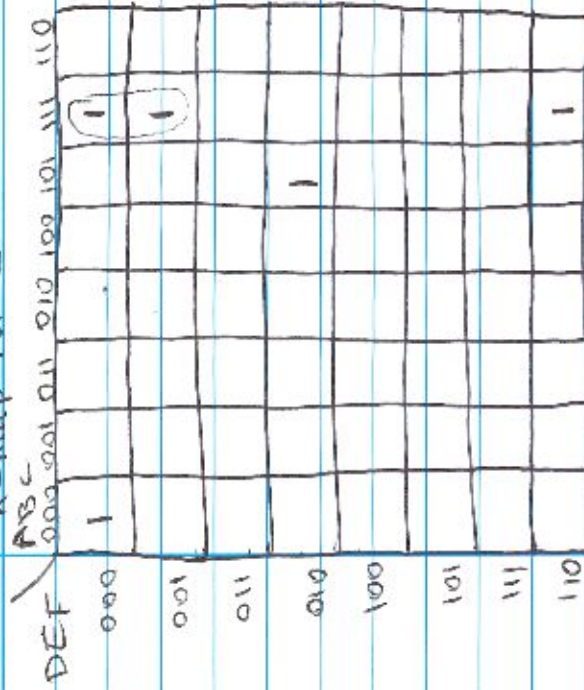
Q3(c)(i)

Question No.

Examiner Only

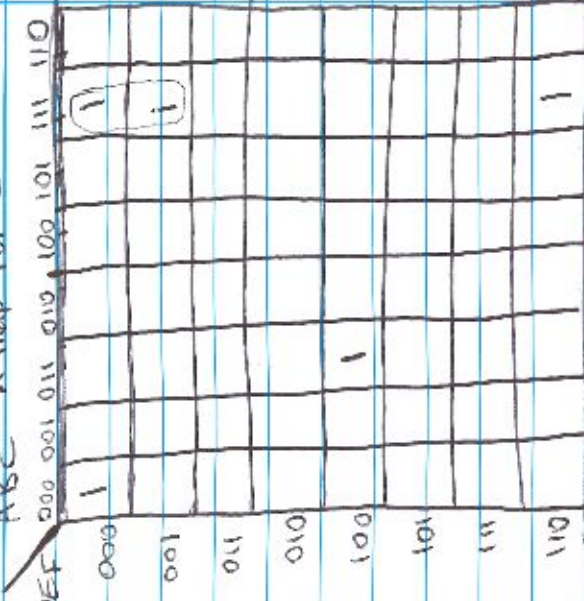
Question No.

Examiner Only

K-map for B^+ 

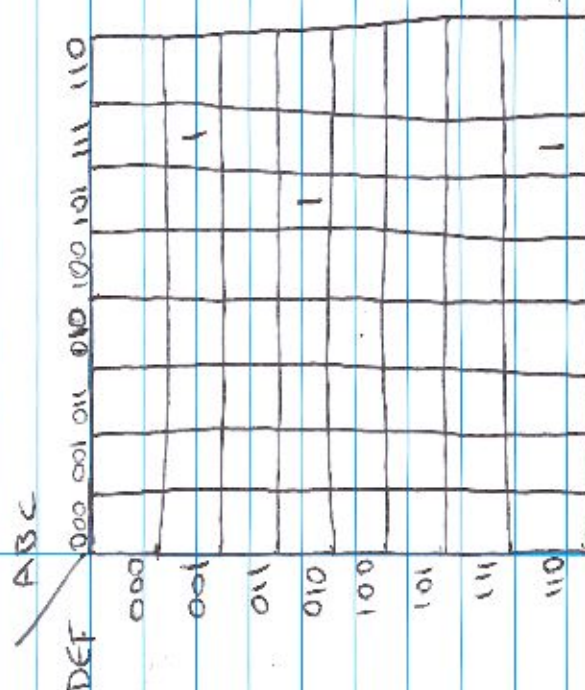
$$B^+ = DB =$$

$$\begin{aligned}
 & NA \cdot NB \cdot NC \cdot ND \cdot NE \cdot NF + \\
 & A \cdot B \cdot C \cdot ND \cdot NE + \\
 & A \cdot NB \cdot C \cdot ND \cdot E \cdot NF + \\
 & A \cdot B \cdot C \cdot D \cdot E \cdot NF
 \end{aligned}$$

K-map for C^+ 

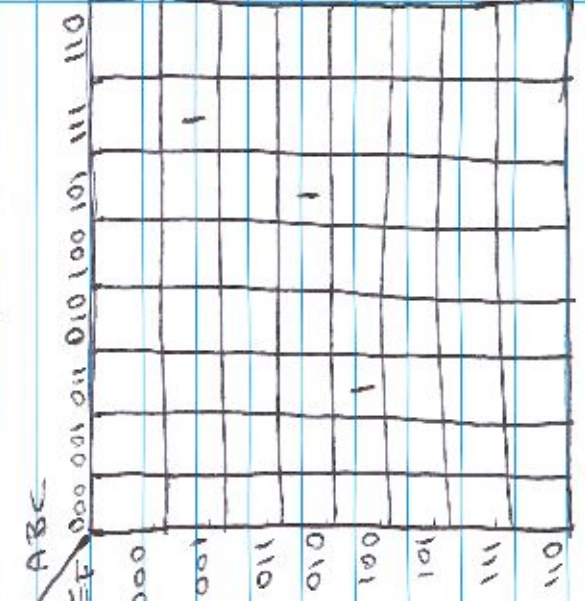
$$C^+ = DC =$$

$$\begin{aligned}
 & NA \cdot NB \cdot NC \cdot ND \cdot NE \cdot NF + \\
 & A \cdot B \cdot C \cdot ND \cdot NE + \\
 & NA \cdot B \cdot C \cdot D \cdot NE \cdot NF + \\
 & A \cdot B \cdot C \cdot D \cdot E \cdot NF
 \end{aligned}$$

K-map for D^+ 

$$D^+ = DD =$$

$$\begin{aligned}
 & A \cdot B \cdot C \cdot ND \cdot NE \cdot F + \\
 & A \cdot NB \cdot C \cdot ND \cdot E \cdot NF + \\
 & A \cdot B \cdot C \cdot D \cdot E \cdot NF
 \end{aligned}$$

K-map for E^+ 

$$E^+ = DE =$$

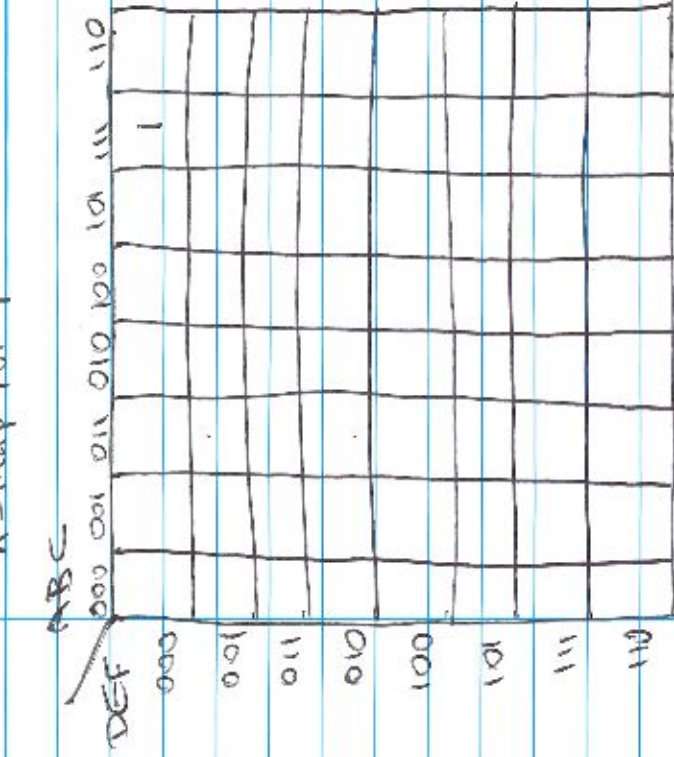
$$\begin{aligned}
 & A \cdot B \cdot C \cdot ND \cdot NE \cdot F + \\
 & A \cdot NB \cdot C \cdot ND \cdot E \cdot NF + \\
 & NA \cdot B \cdot C \cdot D \cdot NE \cdot NF
 \end{aligned}$$

Q3(c)(i)

Question No.

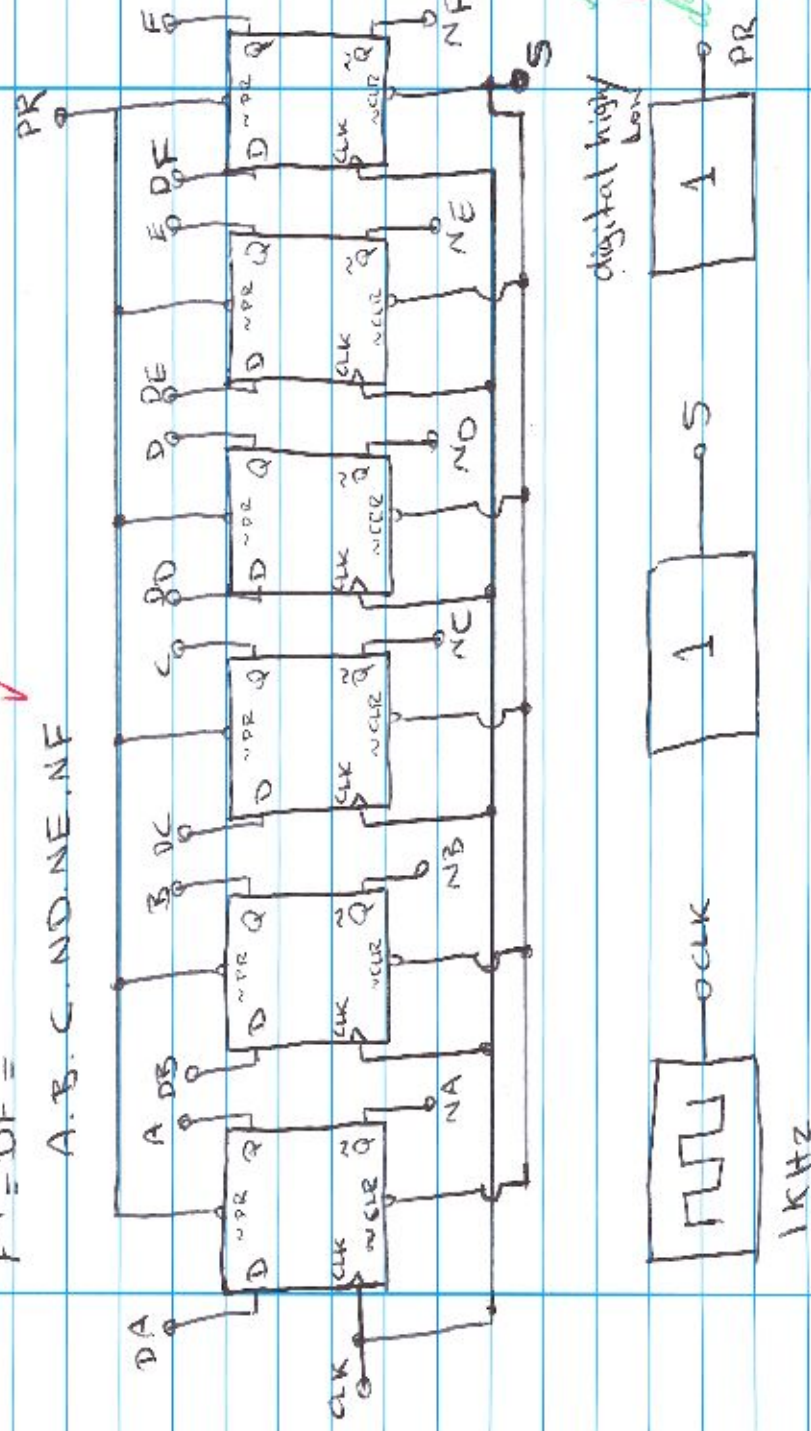
Examiner Only

Examiner Only

K-map for F^+ 

$$F^+ = DF =$$

$$A \cdot B \cdot C \cdot ND \cdot NE \cdot NF$$



Q3(c)(ii)

Apply a seed value of 000000 via high/low signal transition on CLR input of the flip-flops.

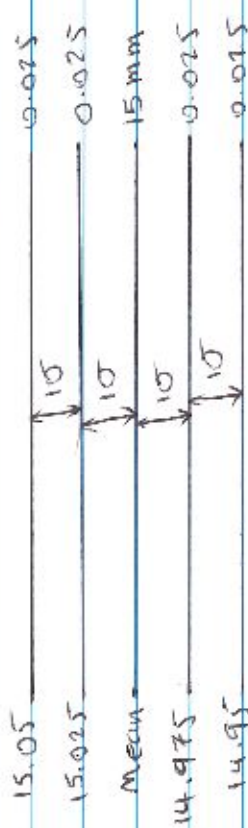
Answer yn unig

Rhify Cwestiwn

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52

Question No.	Examiner Only	Question No.	Examiner Only
Q2 (a)	Mean = 15 mm Range = ± 0.05 mm (i) Standard deviation (std) = $\frac{\text{Range}}{\text{sigma level}}$ $\text{std} = \frac{0.05}{2} = 0.025$ ✓  i. Upper limit = 15.05 ✓ Lower limit = 14.95 ✓ (ii) A process is capable when $CP > 1$ at six sigma process $CP = \frac{\text{Upper spec} - \text{Lower spec}}{6\sigma}$ $CP = \frac{15.05 - 14.95}{6 \times 0.025} = 0.66$ ✓ i. The process is not capable as CP is lower than 1 ✓ at 3 sigma level $\text{std} = \frac{0.05}{3} = 0.166$ $CP = \frac{15.05 - 14.95}{6 \times 0.166} = 0.1004$ ✓ TBL $\Rightarrow$	Q2 (a) (iii) This means:- a six sigma process is basically the product's quality goal, where sigma is statistical measure of variability. In a six sigma system where six sigma is required the standard deviation is to be no more than one twelfth of the mean, that is six standard deviation on either side of the mean. If six sigma fits on upper limit or lower limit of the mean the process is said to be capable if not then it is not capable ✓ Q2 (B) (i) $\text{std} = \frac{0.05}{4}$ $\text{std} = 0.0125$ ✓ That is four standard deviation on either side of the mean i. Upper limits would be:- 15.0125, 15.025, 15.0375 and 15.05 ✓ Lower limits would be:- 14.9875, 14.975, 14.9625 and 14.95 ✓ for rest of Q2 PTO $\Rightarrow$	
Arthur yu unig	Arthur yu unig	Arthur yu unig	Arthur yu unig

Question No.	Examiner Only	Question No.	Examiner Only
Q2(B) (ii)	Capability index which is just a simple number which measures how close a process is running to its specification limits relative to natural variability of the process. The larger the index the less likely any of the items will go outside of its specifications. $Cpk = \min \left(\frac{\text{mean} - L \text{ spec}}{3\sigma}, \frac{U \text{ spec} - \text{mean}}{3\sigma} \right)$ $Cpk = \min \left(\frac{15.02 - 14.95}{3 \times 0.0125}, \frac{15.05 - 15.02}{3 \times 0.0125} \right)$ $Cpk = \min (1.86, 0.8)$ The process can no longer operate at 4 sigma level because according to 3σ rules, 3σ will only fit 0.8 times above mean and 1.86 times below mean. Either side of the mean must be greater than 1 for the process to be capable.	Q1(a)	Compliance testing of electronic products includes emission test, immunity test and safety test. ✓ The emission test ensures that a product is not emitting harmful electromagnetic interference in communication and power line. Electromagnetic compatibility (EMC) is part of compliance test and is ability of a system to operate at its intended environment and without suffering unacceptable degradation in performance due to coupling from other systems or causing unacceptable degradation in performance of other systems via coupling. ✓ Immunity test ensures that a product is immune to common electrical signals from other system such as electromagnetic radiation from radio station and voltage spikes from power line. Safety test ensures that a product is not causing safety risks in situations such as failed or shorted power supply or covered cooling vent. Compliance testing in electrical and electronic products are necessary to enter the global market. Certification are required to satisfy the market requirement. It gives customer assurance that the products are safe to use.
Q2(B)(iii)	The capability (Cp) remains the same because the standard deviations remain the same. Note of the attributes in Cp calculation will change due to change in mean value. Cp calculation takes into account the shift in the mean and compares the results with 3σ rules, that is 3 standard deviation on either side of the mean and if the results are < 1 then the process is said to be not capable. Confused with Cp + Cpk.		
Q2(b)(iv)	The capability (Cp) remains the same because the standard deviations remain the same. Note of the attributes in Cp calculation will change due to change in mean value. Cp calculation takes into account the shift in the mean and compares the results with 3σ rules, that is 3 standard deviation on either side of the mean and if the results are < 1 then the process is said to be not capable. Confused with Cp + Cpk.		

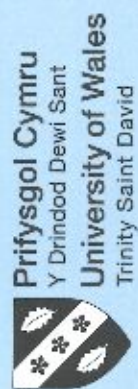
Question No.	Examiner Only	Question No.	Examiner Only
Q1(b)	critical components:- PC cover, power supply and main CPU non-critical components ✓ CD drive, floppy disk, hard drive, memory cards, monitor and keyboard and mouse. ✓ PC cover: ~~not~~ critical because it may block the cooling vent and it should not be conductive. ✓ Power supply:- filtration required to eliminate the spikes and clips from power line. ✓ Most of non-critical products are PC are external and operate with 5V supply from the PC. If: if the critical items are safe the non-critical can be safe. ✓ ESD builds up when two different materials are rubbed together. one of the materials becomes positively charged and the other one becomes negatively charged. for example if walking on a ~~very~~ nylon carpet the person becomes positively charged and they can earth themselves on the ground and can get an electrical shock by touching metal door handle. ✓	Q1(c) (ii)	electrostatic when the charged up at ~~ESD~~ gets in contact with right materials an ESD ~~even~~ occurs. for example when charges applies to an electronic product such as expansion card, the intense heat from the charge can melt or vaporise the tiny components within the device ^{1/2} ✓ and cause a fail to the device. ✓ The types of damage it can cause can be categorised as follow:- Latent damage:- when the item is not completely damaged and it can be functional but it will fail over a period of time. ✓ Catastrophic failure:- where the item is completely damaged during production which has advantage ³ ✓ for manufacturer to identify the damage right away. The disadvantage is that the product is completely damaged and ~~un~~ functional. ✓ For Q1(c)(iv) PTO ⇒
Q1(c) (i)		Q1(c) (iii)	

Q1(c)
(iv)

Manufacturers of electronic component take every possible ~~precautions~~ precautions to protect devices from ESD and the take care in production, transport and delivery. The worker may wear a wrist band to draw ESD charge to it or they may wear special footwear to transfer the charges to the ground. ³ ~~Another~~ Grounding is another way of protecting against ESD as when you are grounded you are electrically neutral.

Q1(d)

Not answered.



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SURNAME: JONES

FORENAME(S): BR/1A

1	Student Number	1303047/1
2	Title of Examination Paper	ELECTRICAL PRODUCTION & TEST
3	Module Code	PSDE 6018
4	Date and Time of Examination	THURSDAY 10 th MAY 2018 9:30
5	Examination Venue	
6	Seat Number	
7	Number of Answer Books handed in	1

[illegible]

23 a)

- Used due to its simplicity
- As a single fault can be detected then a very high percentage of multiple faults will be detected.
- Single stuck-at fault model applies to all nodes in turn, ~~SAO or SAI~~ i.e. SAO = Node grounded, SAI = Node short-circuit to supply rail ✓
- Total number of circuit faults that must be simulated is $m+1$ where m = number of circuit inputs. ✓
- If a multiple stuck-at fault model is used then each node can have any one of 3 states that will be good, SAO or SAI. ✓
- Total number of faulty circuits requiring simulation is $3^n - 1$ which is impractical for large circuits. ✓
- Fault modelling simplifies the number of tests needed compared to exhaustive testing by typically a factor of 5 or 10. ✓

3 input AND gate function;

a	b	c	a	b	c
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	0
1	1	1	1	1	1

Q3 b) STEP 1 - Reduce tests on individual gates using formula $m+1$ where m = number of circuit inputs. i.e. for a 2 input AND gate, $m=2 \therefore m+1 = 2+1 = 3$. ✓

STEP 2 - SET circuit under test's output to equal circuit output i.e. at extreme of propagation path. ✓

STEP 3 - find redundant test vectors using HEX values. ✓

STEP 4 - Take out values that are equal, no repetition. ✓

STEP 5 - also manipulation process to alter logic conditions thus reduce further reducing test vectors. ✓

c)

TEST No.	A	B	C	D	E	F	A+	B+	C+	D+	E+	F+	Faults detected
1	1	1	1	1	1	0	1	1	1	1	0	0	A, B, C, D, E, F, SA1
2	0	1	1	1	0	0	1	0	1	0	1	0	A, SA1, D, SA0
3	1	0	1	0	1	0	1	1	0	1	1	0	B, SA1, E, SA0
4	1	1	0	1	1	0	0	0	0	0	0	0	C, SA1, D, E, SA0
5	0	0	0	0	0	0	1	1	1	0	0	0	D, E, SA1, Y, SA1
6	1	1	1	0	0	0	1	1	1	0	0	1	F, SA1
7	1	1	1	0	0	1	1	1	1	1	1	0	F, SA0

✓

C) A+

DEF	000	001	011	010	100	101	111	110
ABC	1							
000								1
001								
011								
010								
100			1					
101								
111								
110								

$$A+ = DA = \bar{A} \cdot \bar{B} \cdot \bar{C} \cdot \bar{D} \cdot \bar{E} \cdot \bar{F} + \bar{A} \cdot \bar{B} \cdot \bar{C} \cdot \bar{D} \cdot \bar{E} \cdot \bar{F} + \bar{A} \cdot \bar{B} \cdot \bar{C} \cdot \bar{D} \cdot \bar{E} \cdot \bar{F} + A \cdot B \cdot C \cdot D \cdot E \cdot F$$

B+

DEF	000	001	011	010	100	101	111	110
ABC	1							
000								1
001								
011								
010								
100								
101								
111								
110								1

$$B+ = DB = \bar{A} \cdot \bar{B} \cdot \bar{C} \cdot \bar{D} \cdot \bar{E} \cdot \bar{F} + \bar{A} \cdot \bar{B} \cdot \bar{C} \cdot \bar{D} \cdot \bar{E} \cdot \bar{F} + \bar{A} \cdot \bar{B} \cdot \bar{C} \cdot \bar{D} \cdot \bar{E} \cdot \bar{F} + A \cdot B \cdot C \cdot D \cdot E \cdot F$$

C+

DEF	000	001	011	010	100	101	111	110
ABC	1							
000								1
001								
011								
010								
100			1					
101								
111								
110								1

$$C+ = DC = \bar{A} \cdot \bar{B} \cdot \bar{C} \cdot \bar{D} \cdot \bar{E} \cdot \bar{F} + \bar{A} \cdot \bar{B} \cdot \bar{C} \cdot \bar{D} \cdot \bar{E} \cdot \bar{F} + \bar{A} \cdot \bar{B} \cdot \bar{C} \cdot \bar{D} \cdot \bar{E} \cdot \bar{F} + A \cdot B \cdot C \cdot D \cdot E \cdot F$$

c)

DEF	ABC	000	001	011	010	100	101	111	110
000								1	
001									
011									
010									
100									
101									
111									
110									

$$F = 00 = A \cdot \bar{B} \cdot \bar{C} \cdot \bar{D} \cdot E \cdot \bar{F} + A \cdot B \cdot C \cdot \bar{D} \cdot \bar{E} \cdot F + A \cdot \bar{B} \cdot C \cdot D \cdot E$$

mistake 0.5

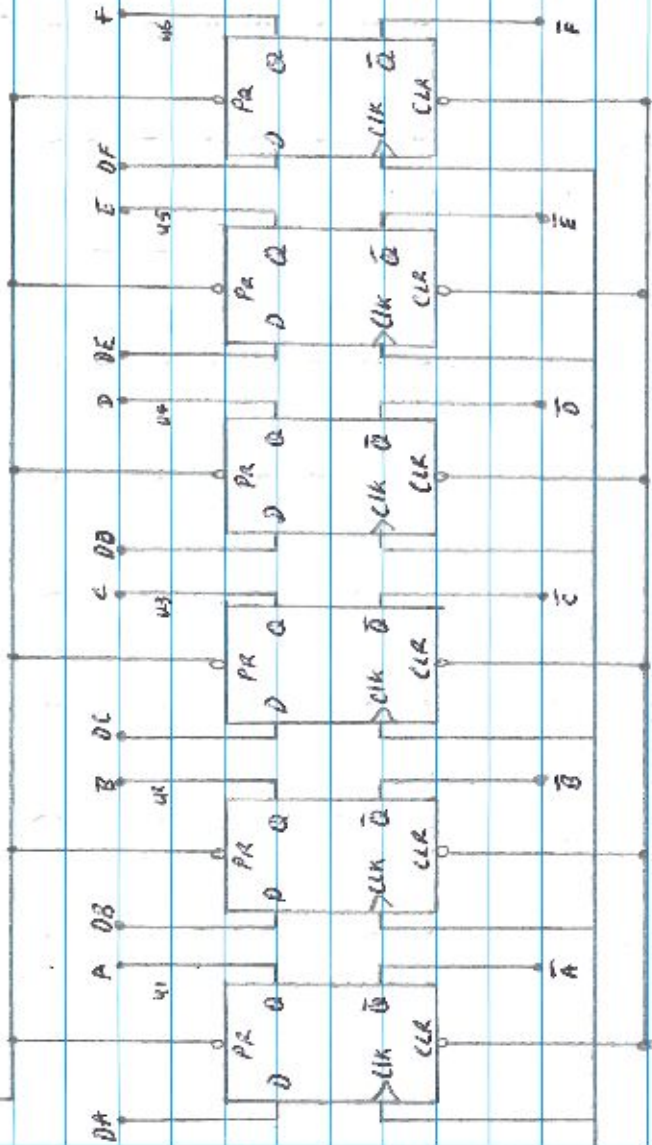
DEF	ABC	000	001	011	010	100	101	111	110
000									
001								1	
011									
010									
100									
101									
111									
110									

$$F = 01 = \bar{A} \cdot B \cdot C \cdot D \cdot \bar{E} \cdot \bar{F} + A \cdot \bar{B} \cdot C \cdot \bar{D} \cdot E \cdot \bar{F} + A \cdot B \cdot C \cdot \bar{D} \cdot E \cdot F$$

DEF	ABC	000	001	011	010	100	101	111	110
000									
001								1	
011									
010									
100									
101									
111									
110									

$$F = 0F = A \cdot B \cdot C \cdot \bar{D} \cdot \bar{E} \cdot \bar{F}$$

i)



1kHz CLK

c ii)

Applying a 'seed' value '5' '000000' via a high to low transition on the 'CLR' input to the Flip Flops.

4) a)

The stream of bits being transmitted is modified the value fed to the LFSR. The final CRC value stored in the LFSR is the checksum and is dependent on every bit in data stream.

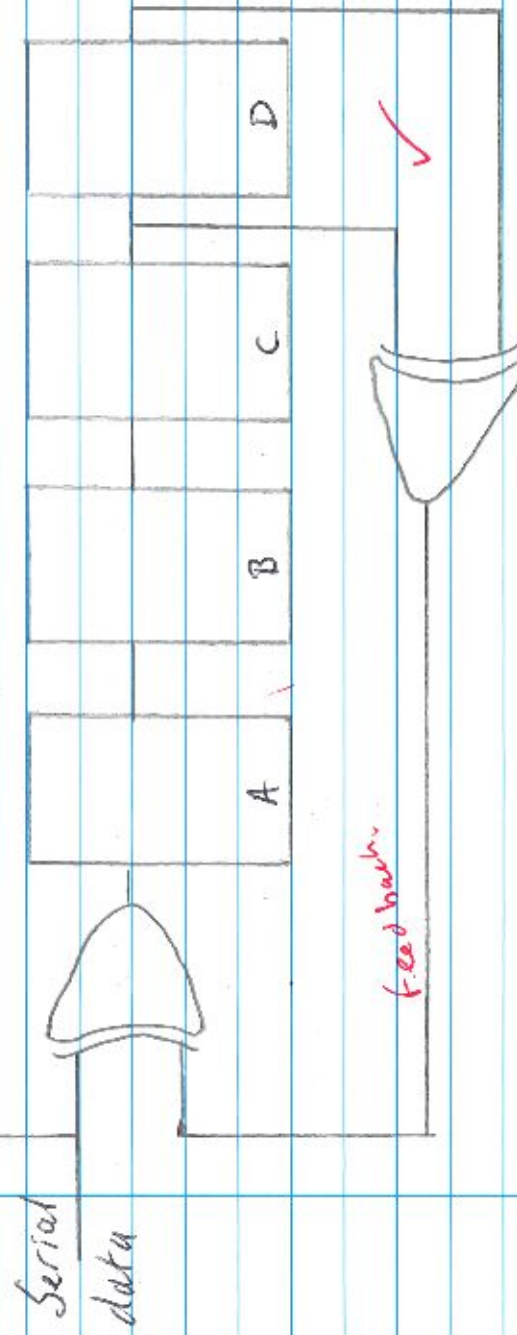
Following data bits transmitted, transmitter sends own checksum to the receiver. The receiver contains same CRC as it run it through the same LFSR setup generating the checksum.

The checksum from the transmitter and receiver is compared for errors, thus determining corruption of data during transmission. Very efficient error detection as small number of bits transmitted in addition to data.

b)

Serial data

D-type Flip Flops.



In reality, a 4-bit CRC calculator would not be considered sufficient in providing transmitted data. This is due to a 4-bit LFSR only having 16 unique values available. With multiple errors, error masking

could occur thus producing 2 identical checksums, increasing the bits reduces the probability to zero thus generally 16-bits are used giving 265K unique values.

$$G(x) = 1 + x^2 + x^4 + x^5 + x^8 + x^{10} + x^{12} + x^{13} + x^{14} + x^{15}$$

$$P(x) = 1 + x^3 + x^4$$

$$\frac{G(x)}{P(x)} = Q(x) + \frac{R(x)}{P(x)}$$

$$G(x) = Q(x) \cdot P(x) + R(x)$$

An LFSR carries out polynomial division on the input of a data stream by characteristic polynomial.

Hence producing an output corresponding to Quotient $Q(x)$ with a Remainder $R(x)$.

This is illustrated using MODULO-2 division of a bit stream.

d)

1/p data	1/p to Reg	new reg value A B C	output
1	1	0 0 0	0
0	0	1 0 0	0
1	1	1 0 1	0
0	1	1 0 1	0
1	0	0 1 1	1
1	0	0 0 1	0
0	0	0 0 0	1
0	1	1 0 0	0
1	0	0 0 0	1
0	0	0 1 1	0
1	1	1 0 0	1
1	1	1 0 0	0
0	0	0 0 0	0
0	0	0 0 0	1
1	1	1 0 0	0
1	1	1 0 0	0
1	1	1 0 0	0
1	1	1 0 0	0

What is the output?

e)

$$G(x^2) = 1010010100101111$$

1/p data	1/p to Reg	new reg value A B C	O/P
1	1	0 0 0	0
0	0	1 0 0	0
1	1	0 1 0	0
0	1	1 0 1	0
0E	1E	1E 1 0	1
1	0	0 1E 1	0
0	0	0 0 1E	1
1E2	1E2	1E2 0 1E	1
0E3	1E3	1E3 1E2 0	1E
0	0	0 1E3 1E2	0
1	0	0 0 1E3	0
0	0	0 0 0 1E3	1E2
1	0	0 0 0 0	1E3
1	1	1 0 0 0	0
1	1	1 1 0 0	0
1	1	1 1 1 0	0

f)

Single bit data stream produces error, multiple errors could produce error masking there for increasing to 16-bit LFSR will reduce the probability.

Question No. 2	Examiner Only	Question No. 2	Examiner Only
a) i)	Mean = 15mm Range = ± 0.05mm $\therefore$ Standard deviation (STD) = $\frac{\text{Range}}{2}$ $= \frac{0.05}{2}$ $= 0.025\text{mm}$ ✓ Upper limit Mean Lower limit Upper limit = 15.05mm Lower limit = 14.95mm. ✓	b) i) STD = $\frac{\text{Range}}{4} = \frac{0.05}{4} = 0.0125$ ✓ Upper limit = 15.0125, 15.025, 15.0375, 15.05mm ✓ Lower limit = 14.9875, 14.975, 14.963, 14.95mm. ✓	1 ✓ 12
i) ii)	6σ is a process quality goal, where sigma statistical measure of variability of a process, where 6σ requires a process STD to be no more than 1/2 the additional spread i.e. 6 x STD either side of the mean. If 6σ fits into the upper & lower limits either side of mean, it said to be 'capable' (>1) if outside these limits it said to be 'not capable' (<1)		
ii)	$C_p = \frac{\text{upper limit} - \text{lower limit}}{6\sigma}$ $= \frac{15.05 - 14.95}{(6 \times 0.025)} = 0.6$ ✓ $\therefore < 1$ not capable. explanation!		3
Arholwr yn unig	Arholwr yn unig	Arholwr yn unig	Arholwr yn unig

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Complete, fold and seal
(see note 2 below)

SURNAME: Callaghan

FORENAME(S): Rhianon

1	Student Number	130 274 0/1
2	Title of Examination Paper	Electronic Production and Test
3	Module Code	PSDE 6018
4	Date and Time of Examination	10/15/18 9:30am
5	Examination Venue	Colleg Sir gar Graig
6	Seat Number	
7	Number of Answer Books handed in	1

List the numbers of the questions you have attempted	Office Use
1	25 1/2
3	14
4	23
Office Use	61%

1 Question 1

- a) Compliance testing includes emissions tests, immunity tests and safety tests ✓
Emissions tests ensure that the product does not emit harmful electromagnetic interference in communications or power lines. Electromagnetic compatibility (EMC) testing is part of compliance testing, this ensures that the product can operate in its environment without, ✓
- Suffering unacceptable degradation in performance due to coupling from another system or ✓
- Causing unacceptable degradation to another system via coupling ✓
Immunity tests ensure the product is immune to electrical signals and ~~electro~~ electromagnetic interference that may be in the working environment such as a local radio station ✓
Safety tests ensure a safety risk will not be caused by something such as a shorted or failed power supply. ✓
Compliance testing and CE marks and certificates are needed for access onto the world wide market. This provides assurance to customers that the product meets performance and safety standards ✓

6/10

Question No.	Examiner Only	Question No.	Examiner Only
1c) (i)	Electrostatic charge builds up when two materials are rubbed together. When this happens one becomes positive and the other negative. The positively charged material has static charge. Shoes being rubbed ~~across~~ across carpet builds static charge. ✓	1c)	There are methods of preventing ESD. Wrist straps can be worn by employees to ground themselves, ESD control shoes and mats can be used along with ESD safe tools. ESD bags can be used when storing and transporting boards. ✓
(ii)	ESD occurs when the charged material touches the right material for example a statically charged person touching a metal door knob would cause the charge to jump causing ESD. ✓	1b)	Critical components are those which you need to make the product work, the ones that are harder to change such as Computer case ✓ PSU ✓ Main CPU ✓
(iii)	If this charge were to discharge on an electronic board the intense heat would cause the small components to melt or vaporise causing failure. ✓ The types of damage caused by ESD can be put into two categories 1) Latent damage - This type of damage is not immediate and is hard to detect. This type of damage will cause a performance issue and eventually fail at a later date. 2) Catastrophic failure - This is the immediate failure of a device although the worst type it is better for detection as it can be detected before it is put into a device. ✓		Non-critical are the addition features that can be easily swapped such as Hard drives ✓ CD drives ✓ Monitor ✓ Keyboard & mouse etc. ✓
		1d)	Decibel notation is useful because it offers a way to express ratio of values that could span magnitudes without the need for units. For example $dB = 10 \log (P_1/P_2)$ $dB = 10 \log (10W/5W) = 3dB. ✓$

Question 3

3 The single stuck at fault model is mainly used because of its simplicity. The model works by applying faults to each node of the circuit in turn. It can be shown that if all single faults are detected there is a high percentage ~~chance~~ chance that multiple faults will be detected. The faults are defined as stuck at 1 (short to supply rail) and stuck at 0 (short to ground). If ~~multiple~~ stuck at fault is ~~as~~ n is the number of nodes. If multiple stuck at fault is being used there are 3 potential states for each node, good, S@1 and S@0. The number of faulty circuits requiring testing would be $3^n - 1$. This is impractical for large circuit due to the number of tests required.

The single stuck at fault model can reduce the tests required by 5 to 10. ~~reducing 5-10.~~

AND	OR	OR
111 1	000 0	000 0
011 0	010 1	010 1
101 0	010 1	010 1
010 0	001 1	001 1

Step 1

Insert fault models onto the inputs of each gate in the circuit. Number of tests required is ~~n+1~~ for each gate is $n+1$ where n is the number of inputs.

Determine which fault each test identifies.

Step 2

Determine the propagation path from to an observable node and enter the propagation vector. This can be done as follows if the gate the fault is propagated through is an AND or NAND gate all inputs except to one carrying the fault must be set to 1. If the gate the fault is propagated through is an OR or NOR all inputs except the one carrying the fault must be set to 0. ~~could be done!~~

Step 3

Trace back through the circuit setting the gates to allow steps 1 and 2 to be completed. Note any conditions where various combinations of inputs produce the same output. For example 01, 10 and 11 would all produce a 1 on the output of an OR gate. ~~5~~

Step 4

Use HEX mapping on the inputs and outputs of the test to find duplicate sets tests. Delete repeats.

Step 5

Use the conditions where various input combinations are valid to create valid duplicate tests, ~~be~~ delete the repeats.

Question No.

3c) A⁺

ABC			000	001	011	010	100	101	111	110
DEF	000	001	011	010	100	101	111	110		
000									1	
001										
011										
010										
100				1						
101										
111										
110										1

$$\begin{aligned} DA &= \bar{A}.B.C.D.\bar{E}.\bar{F} \\ &+ A.\bar{B}.C.\bar{D}.E.\bar{F} \\ &+ A.B.C.\bar{D}.\bar{E}.\bar{F} \\ &+ A.B.\bar{C}.D.E.\bar{F} \end{aligned}$$

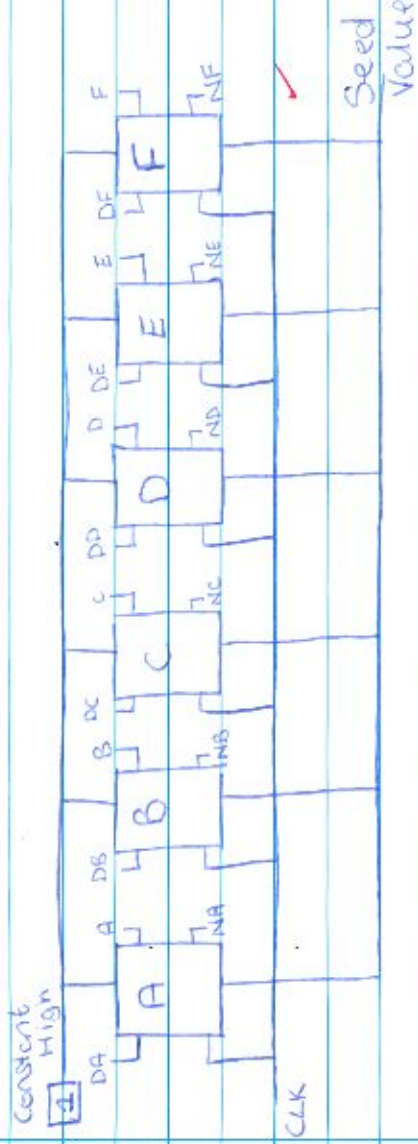
B⁺

000	001	011	010	100	101	111	110
000							
001							
011							
010							
100		1					
101							
111							
110							

Examiner Only

Question No.

3cii)



3cii) 000000 through a high converter X

Arholwr yn unig

Rhify Cwestiwn

Arholwr yn unig

Rhify Cwestiwn

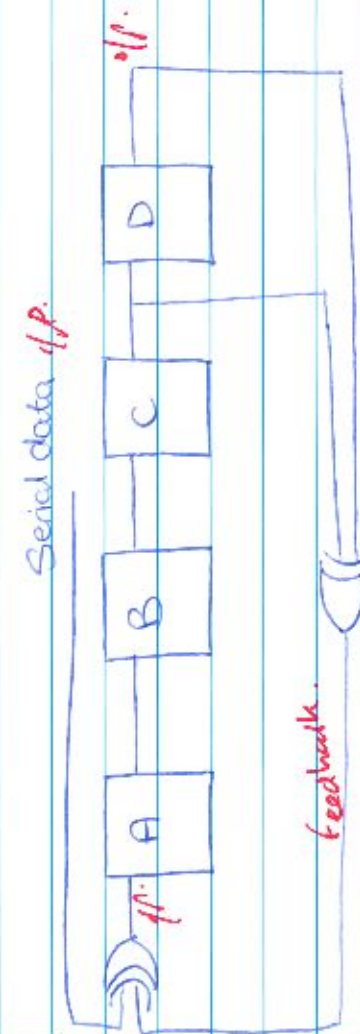
14

Question 4

4

a) The stream of bits transmitted is used to modify the LFSR. The last value in the CRC depends on all bits and is known as the checksum. The transmitter and receiver both have the same checksum as they have been through the same CRC and LFSR set up. Once the data has been transferred the two checksums can be compared for differences. The differences with show data has been corrupt during transfer. *Some missing parts!*

b)



Continued on next page

c) $G(x) / P(x) = Q(x) + R(x) / P(x)$

$$G(x) \cdot P(x) = R(x) + P(x)$$

4d)

Input	Input to Register	AB CD	Output
1	1	0000	0
0	0	1000	0
1	1	0100	0
0	1	1010	0
1	0	1101	1
1	0	0110	0
0	0	0011	1
0	1	1000	1
1	1	1100	0
0	0	0110	0
1	0	0011	0
0	0	0001	1
1	0	0000	1
1	1	1000	0
1	1	1100	0
1	1	1110	0

What is significance of the 0's!

4b

Cont

As this type of CRC only has 4 bits it only has 16 possible unique bits meaning that it is possible that multiple faults will have the same error checksum. For this reason it is a good practice to use a minimum of 16 bits to reduce the chance of having the same checksum.

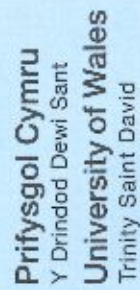
4e) Stream = 1010010100001111

Input	Input to Register	ABCD	Output
1	1	0000	0
0	0	0100	0
1	1	1010	0
0	1	1101	0
0(E1)	1(E4)	(1E1)110 ✓	1
1	0	0(1E1)11 ✓	0
0	0	00(1E1)1 ✓	1
1(E2)	1(E2)	(1E2)00(1E1) ✓	1
0(E3)	0(1E3)	(1E3)(1E2)00 ✓	1E1 ✓
0	0	0(1E3)(1E2)0 ✓	0
1	0	00(1E3)(1E2) ✓	0
0	0	000(1E3) ✓	1E2 ✓
1	0	0000	1E3 ✓
1	1	1000	0
1	1	1100	0
1	1	1110	0

f) To minimise the errors a minimum of a 16-bit CRC should be used this would give over 65,000 unique numbers reducing the chance of masking. ✓

What about the masking!

64K



12 Pages

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FORENAME(S): FREDERICK

SAMES

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1	Student Number	1302738/1
2	Title of Examination Paper	Elec Prog + Test
3	Module Code	PSDE 6018
4	Date and Time of Examination	10/5/18 9:30 am
5	Examination Venue	Girl's Gym Craig
6	Seat Number	
7	Number of Answer Books handed in	

Question 1

- a) Compliance testing is made up of three different testing areas. Emission Testing, immunity testing and Safety testing.

Emission testing is done to ensure that the product does not emit and harmful electromagnetic interference. As this can affect the performance of the product or any thing coupled to it. This interference can come from communication lines  power lines

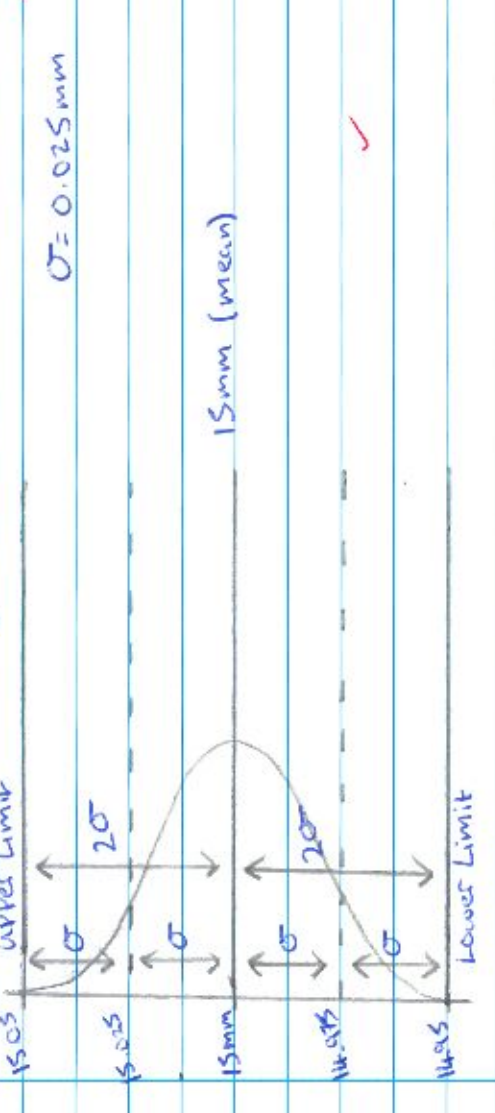
Immunity testing is done to see if the product is immune to interference from other sources. As the interference affects its performance. There are ~~also~~ many sources of EMI, for example power lines or ~~the~~ radio stations. ✓

Safety testing is done to ensure that the part has been designed to meet the Safety Standards and that it is not a risk to the user. For example a shorting power supply or blocked cooling vent can be a risk.

This testing has to be done so that the product can be sold in most world ~~markets~~ wide markets. ✓

doing this testing will provide awareness to possible customers that the product has been designed and built to a good standard. most manufactures will place a Certification mark on the product to show it meets the standards ask for. ✓

Question No.	Examiner Only	Question No.	Examiner Only	Answer yn unig	Rhifyn Cwestiwn
b)	Critical components are components that are seen as critical to the system to operate basic tasks. It is also used as a label for parts that must be as quick to replace in case of damage or failure. normally this is for parts that have to be bespoke made. In a PC this is • PC case • Power supply unit • CPU. Non-critical components are parts that are readily available and are quick and easy to change. also this for parts that if fail will not stop the entire system working • Memory • add on cards • CD drive • floppy drive • monitor • keyboard/mouse.	iii)	there are two categories of damage caused by ESD. Latent damage - this occurs when a component has ~~been~~ had an ESD event on it and the component is still functioning, the only change is a drop in performance. The performance will continue to drop until it eventual failure Catastrophic failure - this occurs in 10-20% of electrostatic discharge events, this is when a component completely fails with no response, this is worst case. The best case after is that the component is identified as faulty before being placed in any equipment iv) In the manufacture of components that are sensitive to electrostatic, great care is taken by the manufacturers to prevent the chances of an ESD event occurring on the component during manufacture, testing, shipping and handling. For the manufacture and testing the employees are made to wear grounding wrist bands, these ground and static before it can be passed to the component. also they must wear non-static PPE and stand on non-static floor mats so as little static is generated are possible For shipping and handling the components are wrapped in non-static materials to protect them from direct contact with static.		
c)	i) Electrostatic charge is built up when two different materials are rubbed together, this causes one material to be positively charged and the other is negatively charged. The positively charged material holds the static. For example this happens when a person rubs socks on carpet the person/cloths become positively charged. ii) An electrostatic discharge occurs when a positively charged material comes in close contact with a negatively charged or grounded material. For electrostatically sensitive components this can cause some serious damage. For example a PLC module card, this component contains many small solder joints. During a ESD event there is a lot of heat generated, this can damage the joint by melting them or even vaporising them completely. This would cause the PLC card to fail				

Question No.	Examiner Only	Question No.	Examiner Only
d) Decibel notation is a convenient way of expressing ratios that may or may not span orders of magnitude. This allows use to express ratios regardless to the input units as it is displays as a dB unit. for example with a power ratio $10 \log(P_2/P)$ is used if we as that we are receiving a power of 10w against a specification of 5w then $\text{Power ratio} = 10 \log(10/5) = 3 \text{ dB}$ or if we receive a power of 5w against a specified value of 10w then $\text{power ratio} = 10 \log(5/10) = -3 \text{ dB}$		Question 2 a) i) mean = 15mm range = ±0.05 Standard deviation (2σ) = range / 2 = $0.05/2 = 0.025$  ii) $C_p = (U_{spec} - L_{spec}) / 6\sigma$ $C_p = (15.05 - 14.95) / 6(0.025)$ $C_p = 0.6$ as can be seen C_p is 0.6, this is less than 1 so it must be said that the process is not capable. <u>3-sigma</u> $STD = 0.05 / 3 = 0.016$ $C_p = (15.05 - 14.95) / 6(0.016)$ $C_p = 1.04$ as can be seen at 3-sigma the C_p value is more than 1 So the process will be capable with 3-sigma	

iii) 6 sigma is a form of quality goal, this will say the probability of a ~~process~~ producing parts within spec. The standard deviation must be one-twelfth of the total allowable spread for it to be classed as capable. other words 6 sigma must fit both sides of the mean to the limits. If the Capability method value is equal to or greater than 1 then the process is said to be capable & if it is ~~the~~ less than 1 then it is not capable. ✓

b)

i) Mean = 15.02

Range = 0.05

$$STD (4 \text{ Sigma}) = 0.05/4 = 0.0125 \text{ mm}$$

Upper Limit = 15.0125, 15.025, 15.0375, 15.05 mm ^{not}
 Lower Limit = 14.9875, 14.975, 14.9625, 14.95 mm ^{changed}

$$ii) Cpk = \frac{\min}{\max} (\text{mean} - L_{\text{spec}}/3\sigma, U_{\text{spec}} - \text{mean}/3\sigma)$$

$$Cpk = \min(15.02 - 14.95/3(0.0125), 15.05 - 15.02/3(0.0125))$$

$$Cpk = \min(1.86, 0.8)$$

$$Cpk = 0.8$$

iii) as can be seen $Cpk = 0.8$ as this is less than 1 we must say that with the shift of the mean the process is not capable. ✓ ^{According to 70 rule!} ~~not capable at the 40 level!~~

iv) The reason the Capability ratio (cp) is not a suitable tool when the mean has shifted is that it does not take the shift value (New mean) into account unlike the Cpk as this is within the calculation for the index value. ^{why?}

Question 3

a) The standard 'Single stuck at' fault model is used to test every input to ensure it has not been shorted to the supply (stuck on - Logic 1) or shorted to the ground (stuck off - Logic 0). This method of testing is used to reduce test vectors that are repeating the same outcomes. For a gate the number of vectors to test is $n+1$ (n being the number of inputs to the gate). The test vectors for a AND and OR gate can be seen below. ✓

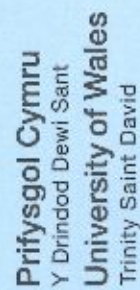
AND		OR	
ABC	Q	ABC	Q
1 1 1	1	0 0 0	0
0 1 1	0	1 0 0	1
1 0 1	0 ✓	0 1 0	1 ✓
1 1 0	0	0 0 1	1

b) Step one is to create individual vector tables per gate using the $n+1$ gate rule. ✓

Step two is to enter the vectors into a test vector table, for this the inputs that are not being tested will have to be set to achieve the expected result. For example U3A, the output from U3A will have to be 1 so its inputs will have to be set to reflect this. ?

Step three each test vector will have an hex value so any vectors with matching Hex values can be cut down to one. ✓

Finally any don't care state inputs can be changed to match other test as long as the output is not changed. This is done to match Hex values so more can be deleted. ✓



12 Pages

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SURNAME: COLES

FORENAME(S): JOS HUA

WARREN IDWAL

GILMOUR

1	Student Number	1303253/1
2	Title of Examination Paper	ELEC. PRODUCTION AND TEST
3	Module Code	PSDE6018
4	Date and Time of Examination	10/5/18 9:30-12:00
5	Examination Venue	
6	Seat Number	
7	Number of Answer Books handed in	

[illegible]

(Gweler yr ochr arall am y fersiwn Cymraeg)

a)

Single stuck at fault models are primarily used because of their simplicity. It shows that if all single stuck at faults are detected, then a high percentage of multi-stuck at faults will be detected. The faults are defined as stuck-at-zero (SA0: shorted to ground) or stuck-at-one (SA1: shorted to supply rail). The number of tests carried out is $n+1$ where n is the number of nodes in the circuit. ✓

If the multi-stuck-at fault model is used then each node can have one of three states: Good, SA0 or SA1. The number of faulty circuit tests required is $3^n - 1$. This is inefficient for larger circuits because of the number of nodes. Compared to the exhaustive testing, the stuck at fault model can reduce the number of tests by a factor of 5 to 10. ✓

Three Input 'AND' | Three Input 'OR'

INPUTS			OUTPUT	INPUTS			OUTPUT
A	B	C	X	A	B	C	X
1	1	1	1	0	0	0	0
0	1	1	0	1	0	0	1
1	0	1	0 ✓	0	1	0	1 ✓
1	1	0	0	0	0	1	1 ✓

number of tests for both = $n+1 = 3+1 = 4$. ✓

3

b) Step 1

INSERT A FAULT model onto the input of each gate. The number of tests required is $n+1$, where n is the number of inputs. Identify the fault that each test locates.

Step 2

Identify the propagation path to an observable node and insert a propagation vector. This is done as follows: If the gate function is an 'AND' or 'NAND' set all the inputs to 1. except for the node that the fault is being propagated through. If the gate function is an 'OR' or 'NOR' set all the inputs to a '0' except the node that the fault is being propagated through.

Step 3

Identify the gate inputs required to achieve steps 1 and 2. Observe multiple conditions of varying inputs that achieve the desired output. For example: to achieve a '1' output on a two input OR gate inputs 01, 10 or 11 achieve the desired output and are all valid.

3

b) - continued

Step 4

Use a hex table to identify repeated tests. Delete the repeated tests and move the fault identifier to the retained test.

Step 5

Observe the multiple conditions of ~~repeated~~ ^{the} varying valid inputs and identify any further repeated tests.

C) i

PRESENT STATE						NEXT STATE					
A	B	C	D	E	F	A ⁺	B ⁺	C ⁺	D ⁺	E ⁺	F ⁺
1	1	1	1	1	0	0	1	1	1	0	0
0	1	1	1	0	0	1	0	1	0	1	0
1	0	1	1	0	1	0	1	0	1	1	0
1	1	0	1	1	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1	1	0	0	0
1	1	1	0	0	0	1	1	1	0	0	1
1	1	1	0	0	1	1	1	1	1	1	0

A⁺ ABC

DEF	000	001	011	010	100	101	110
000	①						①
001							
011							
010			①				
100							
101							
111							
110							

3. c) i - continued

$$A^+ = DA = ABCDEF + \bar{A}BC\bar{D}\bar{E}\bar{F} + \bar{A}BC\bar{D}\bar{E}\bar{F} + \bar{A}BC\bar{D}\bar{E}\bar{F}$$

B+

DEF	ABC							
	000	001	011	010	100	101	111	110
000	1						1	
001								
011						1		
010								
100								
101								
111								
110								1

$$B^+ = DB = \bar{A}BC\bar{D}\bar{E}\bar{F} + \bar{A}BC\bar{D}\bar{E}\bar{F} + \bar{A}BC\bar{D}\bar{E}\bar{F} + \bar{A}BC\bar{D}\bar{E}\bar{F}$$

C+

DEF	ABC							
	000	001	011	010	100	101	111	110
000	1						1	
001								
011								
010								
100								
101								
111								
110								1

$$C^+ = DC = \bar{A}BC\bar{D}\bar{E}\bar{F} + \bar{A}BC\bar{D}\bar{E}\bar{F} + \bar{A}BC\bar{D}\bar{E}\bar{F} + \bar{A}BC\bar{D}\bar{E}\bar{F}$$

D+

DEF	ABC							
	000	001	011	010	100	101	111	110
000							1	
001								
011						1		
010								
100								
101								
111								
110								1

$$D^+ = DD = ABC\bar{D}\bar{E}\bar{F} + \bar{A}BC\bar{D}\bar{E}\bar{F} + \bar{A}BC\bar{D}\bar{E}\bar{F} + \bar{A}BC\bar{D}\bar{E}\bar{F}$$

E+

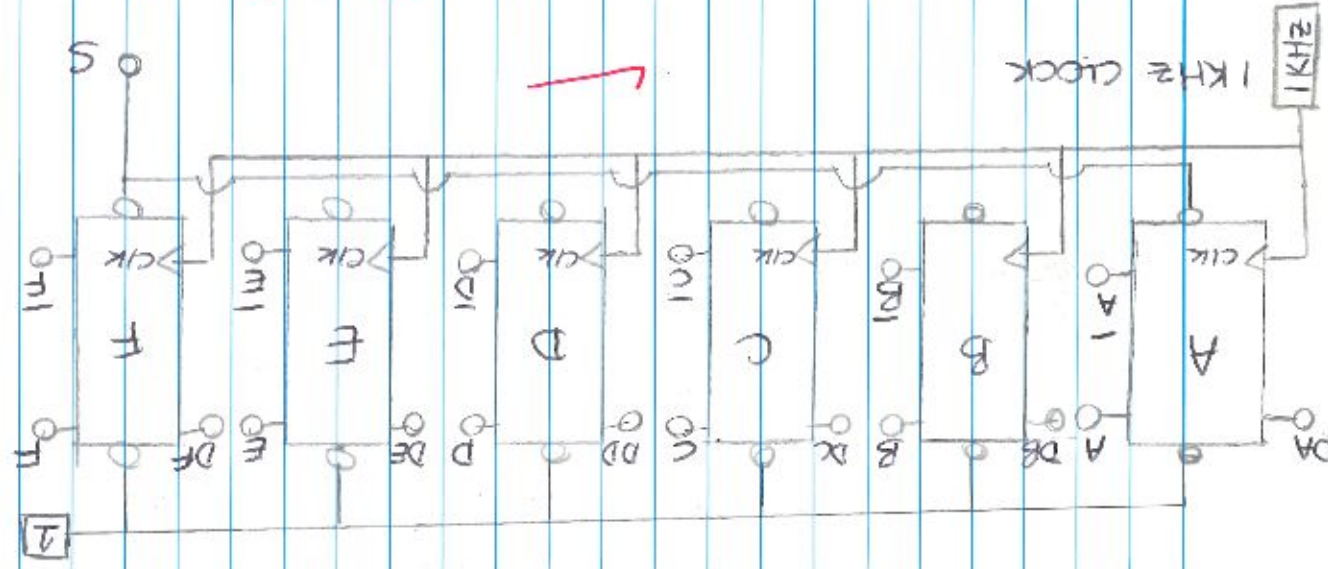
DEF	ABC							
	000	001	011	010	100	101	111	110
000							1	
001								
011								
010			1					
100								
101								
111								
110								

$$E^+ = DE = ABC\bar{D}\bar{E}\bar{F} + \bar{A}BC\bar{D}\bar{E}\bar{F} + \bar{A}BC\bar{D}\bar{E}\bar{F} + \bar{A}BC\bar{D}\bar{E}\bar{F}$$

F+

000	000	001	011	010	100	101	111	110
001							①	
011								
010								
100								
101								
111								
110								

$$F+ = DF = ABC\bar{D}\bar{E}F$$



3c) ii

A seed value of '1's' at 000000 via a high to low signal on the 'CLR' input of the flip-flops. ✓

4

a). an ^{calc} ~~error~~ is used to modify values sent to an LFSR. ✓
 • The final value sent to the LFSR is known as the checksum value, and is dependent on all ~~other~~ bits in the data stream ✓

• After the transmitter has transmitted all the data, it sends a checksum value to the receiver. ✓

• The receiver has an identical CRC because it uses the same LFSR setup, the receiver generates a checksum after all data is received ✓

• The checksum value from the transmitter and receiver are compared to test for data corruption during transmission ✓

• This type of testing is efficient 1A regards to the ^{small} number of bits transmitted with the data. ✓

4 b)



A 4-bit CRC calculator would not be considered in reality because of the lack of unique values. A 4-bit CRC only has 16 unique values. There is a high probability that multiple data errors would create an ideal checksum value and mask the fault. In reality, a 16 bit CRC with 65,536 unique values would be used as the probability for error masking is significantly lower.

c)

$$G(x) = 1 + x^2 + x^4 + x^5 + x^8 + x^{10} + x^{12} + x^{13} + x^{14} + x^{15}$$

$$P(x) = 1 + x^3 + x^4$$

$$G(x)/P(x) = Q(x) + R(x)/P(x)$$

$$G(x) = Q(x) \cdot P(x) + R(x)$$

An LFSR carries out a polynomial division on an input data stream by a characteristic polynomial. The result is quotient $Q(x)$ and remainder $R(x)$.

4 d)

INPUT SERIAL DATA	INPUT TO REGISTER	NEW CRC VALUE	OUTPUT
1	0	0000	0
0	0	1000	0
1	0	0100	0
0	0	1010	0
1	0	1101	0
1	0	0110	1
1	0	0011	0
0	0	0001	1
0	0	1000	1
1	0	1100	0
0	0	0110	0
1	0	0011	0
0	0	0001	1
1	0	0000	1
1	1	1000	0
1	1	1100	0
1	1	1110	0

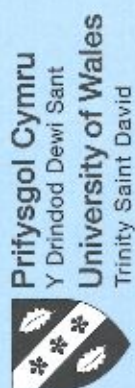
What is the significance of the output?

4
e)

INPUT SERIAL DATA	INPUT TO REGISTER	NEW CRC VALUE	OUTPUT
1	1	0000	0
0	0	1000	0
1	1	0100	0
0	0	1010	0
0	0	1101	0
0 0 0 (E)	1	(1E) 110	1
1 1 (E)	0	0 (1E) 11	0
0	0	0 (E) 0 (1E) 1	1
1	0	0 (E) 0 (1E) 0	1 (E)
1 E 3	1	1 0 0 (E)	0
1	0	0 1 0 0	0 (E)
0	0	0 0 1 0	0
1	0	0 0 0 1	0
1	0	0 0 0 0	1
1	1	1 0 0 0	0
1	1	1 1 0 0	0

Errors not identified at the 4th stage and not corrected. Confusion here!

f) in reality a higher but CRC would be used to prevent error masking. A 16-bit CRC has 65,536 unique values and a far lower possibility of error masking compared to the 4-bit CRC.



Examination Answer Books

12 Pages

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List the numbers of the questions you have attempted	Office Use
1	19
2	31
4	27
Office Use	759

Q2

a) i)

$$\text{Standard deviation} = \frac{\text{Range}}{2}$$

$$= \frac{0.05}{2}$$

$$= 0.025 \text{ mm} \quad \checkmark$$



8

✓

ii)

The capability index (C_p) can be determined by dividing the full range spread by 6σ i.e. 6σ will fit into the range.

$$C_p = \frac{\text{Upper} - \text{Lower}}{6\sigma}$$

$$= \frac{15.05 - 14.95}{6 \times 0.025}$$

$$= \frac{0.1}{1.5}$$

$$= 0.6$$

This process is not capable as C_p is not greater than or equal to 1. ✓

6

✓

iii) The process sigma is a tool used to achieve process quality goals. A process is said to be capable if the standard deviation is no greater than one twelfth of the full spread i.e. 6 standard deviations on either side of the mean. ✓

b) i)

$$\text{Standard deviation} = \frac{\text{Range}}{4}$$

$$= \frac{0.05}{4}$$

$$= 0.0125 \text{ std}$$

The ~~new~~ limits are as follows:

$$\text{Upper} = 15.025, 15.05$$

$$\text{Lower} = 14.975, 14.95$$

no change to limits!

ii)

$$\text{Cpk} = \frac{(\text{Upper} - \text{mean})}{3\sigma} \text{ or } \frac{(\text{mean} - \text{Lower})}{3\sigma}$$

$$= \frac{15.05 - 15.02}{3 \times 0.0125} \text{ or } \frac{15.02 - 14.95}{3 \times 0.0125}$$

$$= \min(0.8, 1.86)$$

The capability index for this system is 0.8 ✓

iii) This indicator that the system is no longer capable at 4σ level. This is because 4 standard deviations will no longer fit between the mean and the upper limit. ✓

iv) The Cpk ratio is not suitable because the ~~ratio~~ range doesn't change. The capability index takes the mean shift into account, and finds the values for the upper and lower tolerances individually. ✓

Q4

a) The stream of data bits are used to verify the ~~var~~ values fed back into the LFSR. The final value obtained is called the checksum.

The transmitter will send its checksum and it has sent all of the data.

The receiver performs its own CRC using an identical LFSR setup.

The two checksums are compared in order to determine whether any error are present; if they match, the system is ~~ok~~ ✓

CRCs are widely used due to their efficiency and the relatively small amount of data that is sent.

b)

Data input stream



Typically, a four bit system will not be employed as there are only 16 possible values it can produce. This does not provide sufficient integrity as ~~there is~~ there is a high chance of a faulty system providing the correct checksum.

Typically, a 16 bit ~~say~~ LFSR is used as it will provide 65536 possible values.

c)

$$G(x)/P(x) = Q(x) + R(x)/P(x)$$

or

$$G(x) = Q(x) \cdot P(x) + R(x)$$

When the serial input sequence $G(x)$ is divided by the characteristic polynomial $P(x)$, a quotient $Q(x)$ and remainder $R(x)$ are found. This can be shown using modulo-2 division (i.e. x-or rather than subtraction).

on values representing the PDS.

d)

LFSR			
Input stream	Input to registers	data ABCD	Output
1	1	0000	0
0	0	1000	0
1	1	0100	0
0	1	1010	0
1	0	1101	0
1	0	0110	1
1	0	0011	0
0	0	0001	1
0	1	1000	1
1	1	1100	0
0	0	0110	0
1	0	0011	0
0	0	0001	1
1	0	0000	1
1	1	1000	0
1	1	1100	0
1	1	1110	0

which is the output sequence?

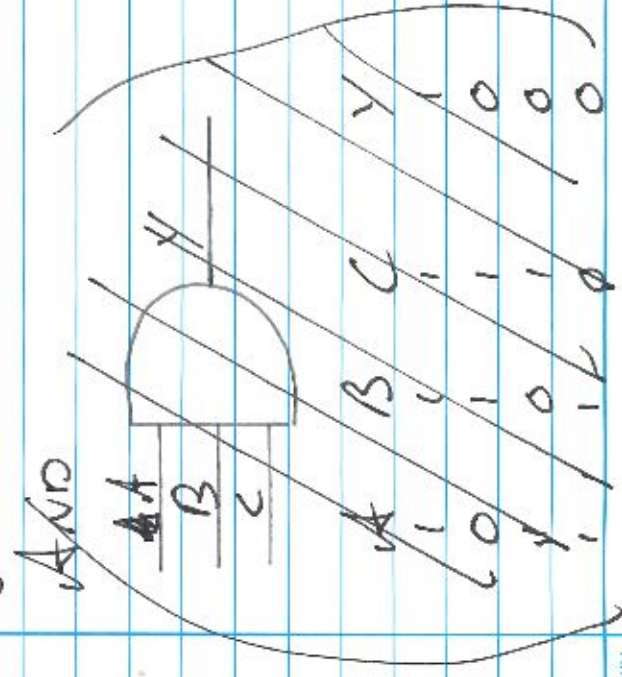
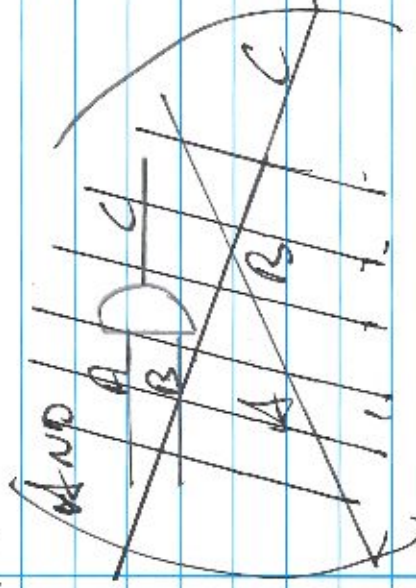
e)

Input stream	input to register	16-bit data ABCD	output
1	1	0000	0
0	0	1000	0
1	1	0100	0
0	1	1010	0
(OE)	(1E)	1101	0
1	0	(1E)110	1
0	0	0(1E)11	0
(1E2)	(1E2)	00(1E)1	1
(OE3)	(1E3)	(1E2)00(1E)	1
0	0	(1E3)(1E2)00	(1E)
1	0	0(1E3)(1E2)0	0
0	0	00(1E3)(1E2)	0
1	0	000(1E3)	(1E2)
1	0	0000	(1E3)
1	1	1000	0
1	1	1100	0
1	1	1110	0

What about matching? ✓

f) When a single ~~error~~ error is present, the output will always show this error. However, multiple errors can be marked at the end of the sequence. In order to ~~see~~ rectify this issue, a 32-bit LFSR can be used. ✓

A fault simulator typically use single stuck at fault models due to the lower number of test vectors required. Multiple fault testing requires $2^n - 1$ number of tests, where n is the number of IC pins. To avoid this can quickly result in too many tests for larger circuits. Single fault testing on the other hand only requires $2n - 1$ tests. This is for fewer tests, and single faults account for the majority of multiple faults.



OR



	A	B	C	Y
0	0	0	0	0
1	0	0	1	1
2	0	1	0	1
3	0	1	1	1
4	1	0	0	1
5	1	0	1	1
6	1	1	0	1
7	1	1	1	1

b)

In order to model the circuit shown in figure 1.1, it is first necessary to insert each individual gate into a truth table as shown below:

(no. tests = 2^n for each gate = 13)

Test No.	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z	Hex	Inputs
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
10	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
12	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
13	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

a)

Compliance testing is necessary to test for emissions, ESD, safety and insulation.

Emissions are important to test because they can have an impact on the environment. ESD is tested because static can cause damage to delicate components. Static discharge can also be dangerous in explosive zones where flammable substances can be ignited. ^{ESD not part of this section!}

Safety is tested because in order to prevent injury to individuals. If someone were to be injured or killed then the company could face heavy fines or legal action. There are many bodies worldwide that test for compliance; these include CE in Europe, the FCC in the USA, and BSI in the UK. If a product has one of their logos it suggests it has been tested for compliance.

Insulation is tested to show that no electrical contact can be made by living beings. ??

c) The reds are moved inserted into the following table

Present state						Next state					
A	B	C	D	E	F	A	B	C	D	E	F
1	1	1	1	1	0						
0	1	1	1	0	0						
1	0	1	0	1	0						
1	1	0	1	1	0						
0	0	0	0	0	0						
1	1	1	0	0	0						
1	1	1	0	0	1						

b) Critical components are those that are essential to the operation of the device. In a PC, these would be:

- PSU ✓
- Motherboard ✓
- RAM ? ✓ *can be critical*
- CPU ✓
- Hard drive ? ✓ *can be critical*
- BIOS ✓ *is a component*

Non-critical components on the other hand are those that the device will work without:

- Monitor *will not cause problem*
- Keyboard
- Mouse
- CD drive
- USB ports ✓
- etc.

c) i)

Electrostatic charge builds up when two different surfaces come into contact. This will result in a build up of charge. An example of this would be if someone were to rub a balloon on their hair. This causes a build up of charges in the balloon.

ii) An electrostatic discharge occurs when a charged surface is ~~open~~ in contact with a surface of opposing potential. This allows a brief flow of current and ~~with~~ as the PD of the two surfaces are balanced. An example of this is when a charged ~~positively~~ charged person touches ground.

Inducted example would be good!

iii) ESD is problematic due to the damage it can cause. There are two types of damage caused by ESD:

Latent damage - Where the discharge is ~~not enough~~ does not cause enough damage to stop the operation of the system, but it will likely succumb to this damage at a later time.

Catastrophic damage - Where the discharge is severe enough to completely wipe out all functions of the device. ✓

Any advanced design designer!

iv) There are numerous methods available to prevent ESD. First of all, there are air mist straps that can ground an individual and prevent static accumulation. It is also possible to entirely ground a work surface. There is anti-static clothing and flooring that can be used to further decrease the build up of static.

It is possible to prevent or reduce the effects of ESD through good design principles and practices. ✓

Example of sensitive business!
and results of ESD damage.

Q1

d) The decibel notation is convenient as it the ratio is kept constant. dB is an example is shown below.

$$\text{gain(dB)} = 10 \log_{10} \left(\frac{10}{5} \right)$$

$$= 3 \text{ dB}$$

$$\text{gain(dB)} = 10 \log_{10} \left(\frac{50}{25} \right) \quad \checkmark$$

$$= 3 \text{ dB}$$

The two equations both start with a gain of two. This can be difficult to see, however, especially with ~~large~~ ^{small} numbers and more complex numbers. The gain in dB is the same in both scenarios, making it easier to read. $\checkmark$

Also Compression and useful when dealing with large pressure values!