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by Alex Williams

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Good list of tables

1. Executive summary

IC fabrication faults occur when developing prototypes and components. Fault modelling can identify these faults. Following research, Automatic Test Equipment methods were found to deliver fast results, allowing the circuit under test (CUT) to be compared against known faults derived from test-vectors. Popular fault models included stuck-at-line faults where an input or output of a logic gate is stuck at logic 1 or logic 0, transistor faults, memory faults and bridging faults.

In the wider engineering field, other test methods available during mass production were noted. Bed-of-nails testing allows for rapid testing of circuitry with spring-loaded pins making connections to PCB boards and testing against known faults. Contact by vacuum allows an automated process for fast, repeatable and reliable results.

Another mass production testing method was machine vision processing. The camera scans the test subject and identifies faults such as missing components, alignment, orientation and colour. Although, it cannot be used to test circuitry it could be paired with other test-methods to eliminate faults.

Electrostatic discharge damages components, the main source being human contact. Preventative measures included operators wearing earth-bonding straps and using antistatic tools.

The CUT was created and simulated on MultiSim using three test-vectors selected from the derived table having reduced faults due to the reduction and wildcard method. This was compared against a word-generator and 6-bit register using an X-OR gate to detect a circuit fault. All tests successfully identified their faults, proving the prototype.

The circuit was then built on Labview and using the DAQ interface board, was tested with the same fault conditions. This highlighted the need to always start with testing no-fault condition as the fault-indicator showed a fault on the first test.

Finally, the circuit was built on CAM software to generate Gerber files for sending to a manufacturer for mass production.

Summary demonstrates a good understanding of the requirements and purpose of the tasks

2. Research

2.1 IC Fabrication Faults

When developing a prototype, different strategies can be used to test the product. Fault modelling is a popular technique used. It allows the designer to model known faults from a truth table and target areas to test. Automatic Test Equipment (ATE) methods can be used which can deliver fast results. This method then allows the circuit under test (CUT) to be compared against the generator faults. Popular fault modules include single stuck-at-faults (SSF), transistor faults, both open and short circuit, delay faults, memory faults, and bridging faults. (Koren & Koren, 1998)

Figure 1 shows an example of some of the fault models.

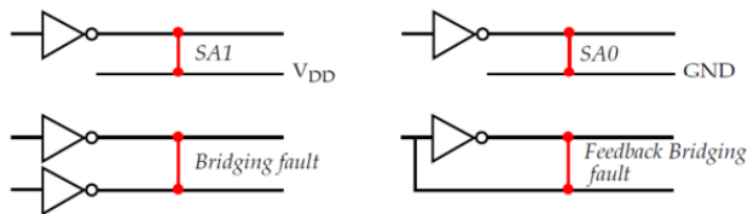


Figure 1: Fault Models (Plusquellic, 2004)

Single stuck-at-faults or line stuck-at-faults are typically when a logic gate has an input stuck at logic 1 or logic 0. This has a direct effect on the output of the circuit. Stuck-at-faults also occur at transistor level where typically a transistor switch will become stuck open or closed. (Ghosh, 2020)

Bridging faults refer to open or short circuits between connections or components within the circuit. When a short occurs between two wires it is also referred to as a bridging fault. (Insight Analytical Labs, 2022)

Faults that occur during manufacturing include processing defects such as missing contacts, parasitic transistors and oxide breakdowns. Material defects such as surface impurities on the chips/boards from ion migration or bulk defects such as cracks and crystal imperfections in lower-level components may also exist. (Hayes, 2002)

Resistive faults are manufacturing defects in integrated circuits. They result in delay faults that cause reliability and timing issues. They are identified by speed tests by checking the silicon at faster speeds than what is required. (Mohammadat, 2015)

Good explanation with examples

2.2 Stuck at Fault Modelling

Single stuck-at-fault (SSF) is the most common modelling technique. This is usually where the logic gate is stuck at logic 0 or logic 1. Characteristics that define SSF are that only one line is faulty, the fault is fixed at high or low logic (1 or 0) and that the fault could be on the input or output of the gate. (Hayes, 2002)

Figure 2 shows a test vector where the input for the AND2 gate is stuck at logic 1 resulting in the output being logic 1 instead of the true response of logic 0.

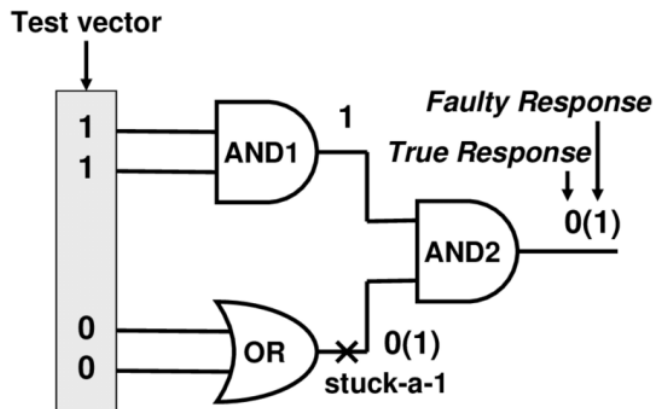


Figure 2: SSF Model (Han & Lee, 2008)

Using SSF methods, the complexity of test procedures can be reduced due to a series of defects being modelled by one stuck at fault logic. This is shown in Figure 3 where two different logic gates can be represented by one test. This is sometimes referred to as fault equivalence. (Ubar, et al., 2017)

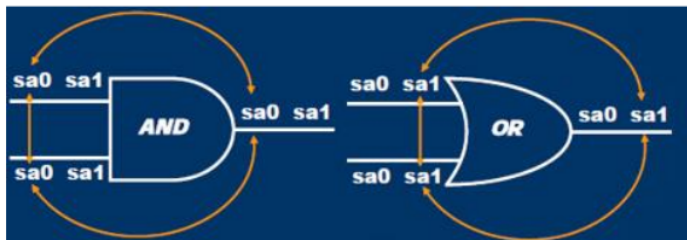


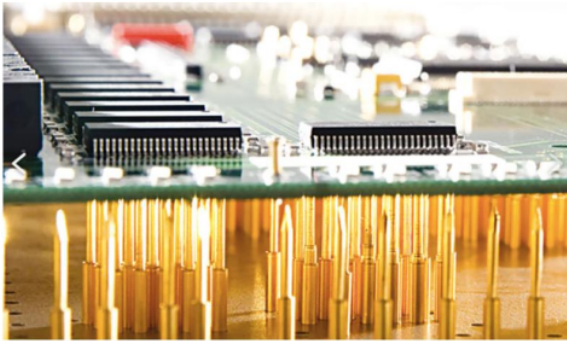
Figure 3: Equivalent SSF (Plusquellic, 2004)

Good research carried out on this topic

2.3 Bed of Nails Testing

A bed of nails test is a traditional electronics test where multiple pins are inserted into a test board and are aligned with a circuit board and connected to measuring units by wires. The device will house an array of spring-loaded pins and each pin will make contact with a node

on the CUT. Pressing the circuit under test down on the bed of nails then creates a reliable contact in fast-time, simultaneously made with hundreds or even thousands of individual test points within the circuitry. The force applied to make the contact can be applied manually but common practice sees a vacuum used for repeatability, accuracy and speed (Professional Plastics, n.d.). Bed of nails are better for testing multiple PCB from larger scale productions rather than wiring into individual breadboards. The test will highlight any manufacturing defects in the PCB and can identify if components are open/short circuit. An example of this test with the spring-loaded pins on show can be seen in Figure 4. (Cockfield, 2019)



Good explanation with relevant example

Figure 4: Bed of Nails Test (Cockfield, 2019)

The bed of nails is a highly successful test method due to its speed and ability to automate with machine control vacuums and as there is no wired connections needed to the board it has a fast throughput capability.

2.4 Machine Vision

According to Cognex, machine vision systems are designed to inspect for “defects, contaminants, functional flaws, and other irregularities in manufactured products.” (n.d., p. 1) The major components of a vision system include lighting to illuminate the part to be inspected, a lens to capture the image, vision processing software to read the image and a communication system to send the communication links. This is often done over a serial connection but modern cameras are integrating Profinet and ethernet features. Applications of vision systems include appearance inspection, positioning, dimensional measurement, presence/absence inspection and text/barcode inspection. (Keyence, n.d.)

Although an expensive initial set up, machine vision can be set up on a production line and scan components as they pass through. This makes it a great testing tool due to its fast-processing time and accuracy in its tests. Machine vision cannot be used to test circuitry on its own, although it can be paired with other test methods to eliminate faults. For example, the machine vision could scan PCB boards for missing chips and orientation. This could stop

already faulty boards going forwards on a production line and saving time by preventing visually faulty boards going for circuitry test on a bed of nails.

2.5 Frequency Signature Analysis

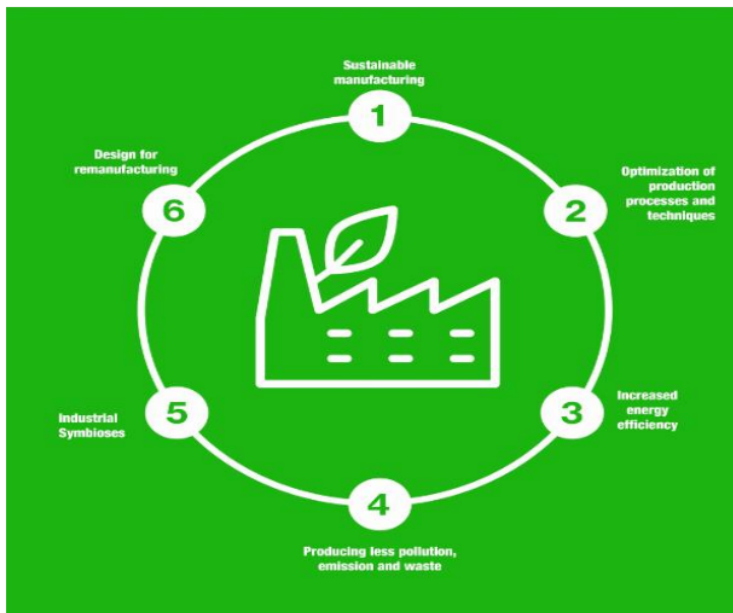
Lee and McCluskey state that “a Failing frequency signature is a collection of the failing frequency of each pattern in a pattern set. A failing frequency is the minimum frequency that indicates an erroneous output when a frequency sweep test is applied” (2008, p. 1). Analysing the frequency signature can then find small-delay defects as any defects in the component shows on the frequency signature. This method allows hard to detect faults in no trouble found devices to be detected effectively with the analysis also being used for characterisation tests. (McCluskey & Lee, 2008)

[An industrial application example should be used here](#)

2.6 Manufacturing Sustainability

Manufacturing testing can be an expensive process with more than 60% of a products cost attributed to testing. This means testing has to be accurate and efficient in order for the product to be sustainable. Whereas tadeonal board level testing such as in circuit test followed by functional test is okay for prototypes and small production, during larger scale manufacturing ATE systems should be considered. (Abadir & Ambler, 2013) When prototypes are designed considerations need to be made around materials used in production, testing and packaging in order to meet the wider goal of sustainable manufacturing. Supply chains should be engaged with the try and eliminate waste and re-use materials across sectors in a localised supply chain where possible and the design should also consider the products end of life and disassembly. (Institution of Mechanical Engineers, 2022)

Products should try to be designed within the sustainable manufacturing closed loop industry. The loop can be seen in Figure 5.



Good coverage on this with relevant points made

Figure 5: Sustainable manufacturing closed loop industry (Jokinen & Marwede, 2017)

2.7 Effects of Electrostatic Discharge

Electrostatic discharge (ESD) is the discharge of static electricity when a connection is made between two objects. (Rouse, 2011) When two insulated surfaces rub together or pull away from each other, electrostatic charge can be created. This results in one surface gaining an electron and the opposing surface losing one (RTP Company, 2020).

Within Integrated circuits (IC), the voltage in electrostatic discharge can be high enough to cause oxide dielectric breakdown and the heat generated from the current can subsequently cause the silicone to melt resulting in short circuits. This damage can be permanent, leaving devices and components damaged and non-repairable. An example of ESD is shown in Figure 6. ESD does not guarantee device/component failure but can cause latency issues within the circuit that will further degrade over the lifetime of the device. (Technofaq, 2018).



Good explanation and example

Figure 6: Electrostatic Discharge Damage on PCB (Technofaq, 2018)

Human contact is a common source of ESD. Different components can withstand a different level of ESD and Table 1 shows examples of how much voltage different components can withstand.

Device type	ESD withstand voltage sensitivity (V) HBM
MR heads, RF FETs	10 - 100
Power MOSFETs PIN diodes, laser diodes	100 - 300V
Pre - 1990 VLSI	400 - 1000V
Modern VLSI	1000 - 3000V
HCMOS	1500 - 3000V
CMOS B Series	2000 - 5000 V
Linear MOS	800 - 4000 V
Small geometry older bipolar	600 - 6000 V
Small geometry modern bipolar	2000 - 8000 V
Power bipolar	7000 - 25000 V
Film resistor	1000 - 5000 V

Table 1: Voltage sensitivity from ESD from human contact (Electrostatic Solutions Ltd, 2012)

2.8 Electrostatic Discharge Prevention

The most common prevention method for circuits to be protected against ESD is grounding to earth. It is common practice in manufacturing plants for operators to have an earthing strap connected to the wrist or ankle in order to remove any static build up in the body by giving it a path to ground. Figure 7 shows an example of an operator using ESD preventative measures.

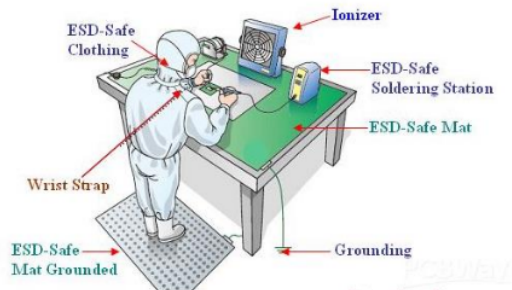


Figure 7: ESD Preventative measures (Das, 2022)

Using best working practices such as operators wearing ESD safe clothing and using antistatic tools, bags, table and floor mats will help reduce the chance of electrostatic discharge. (IMB, 2021)

Relevant preventive measures are covered and explained in good detail, with application example

3. Design of Assignment Requirements

The six-input logic circuit that is used for the circuit under test (CUT) is shown in Figure 8. The data was obtained from the single stuck-at-fault (SSF) model. This identifies and eliminates any redundant/duplicate data in the sequence allowing a great reduction in data and also produces an updated sequence for the test and analysis.

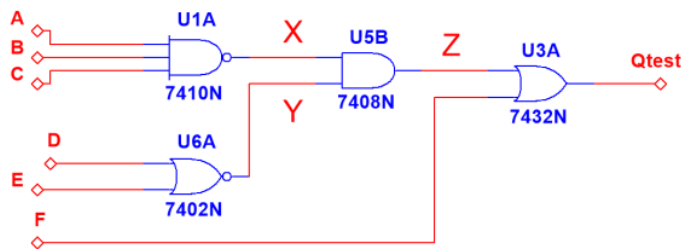
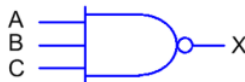


Figure 8: Circuit Under Test

3.1 Stuck at Fault Model Method

The stuck at fault model was used to identify faults where components on the circuit would be stuck at faults at logic 0 (SA0) or stuck at faults at logic 1 (SA1). The test vectors were identified for all the gate and were reduced using the $m+1$ formula. M is the number of gate inputs.

Figure 9 shows an example of a three-input NAND gate with stuck at fault model. As there are three inputs for this example, with the formula applied, it results in 4 test points.



Test No	A	B	C	X
1	1	1	1	0
2	0	1	1	1
3	1	0	1	1
4	1	1	0	1

Figure 9: Test vectors for 3 input NAND gate

Figure 10 shows the test vectors for the 2-input NOR gate.



Test No	D	E	Y
5	0	0	1
6	1	0	0
7	0	1	0

Figure 10: Test vectors for 2 input NOR gate

Figure 11 shows the test vectors and logic for a 2-input AND gate.



Test No	X	Y	Z
8	1	1	1
9	0	1	0
10	1	0	0

Figure 11: Test vectors for 2 input AND gate

Figure 12 shows the test vectors and logic for a 2-input OR gate



Test No	Z	F	Q
11	0	0	0
12	0	1	1
13	1	0	1

SSF reduction methods carried out for each gate and explained using examples

Figure 12: Test vectors for 2 input OR gate

3.2 SSF Test Vectors

The initial truth table for the stuck at fault conditions is shown in Table 2.

Test No	A	B	C	D	E	F	Qgood	HEX	X	Y	Z	Fault
1	1	1	1	0	0	0	0	70	0	1	0	A+B+C SA0
2	0	1	1	0	0	0	1	31	1	1	1	A SA1
3	1	0	1	0	0	0	1	51	1	1	1	B SA1
4	1	1	0	0	0	0	1	61	1	1	1	C SA1
5	0*	0*	0*	0	0	0	1	01	1	1	1	D+E SA1
6	0*	0*	0*	1	0	0	0	08	1	0	0	D SA0
7	0*	0*	0*	0	1	0	0	04	1	0	0	E SA0
8	0*	0*	0*	0	0	0	1	01	1	1	1	X+Y SA0
9	1	1	1	0	0	0	0	70	0	1	0	X SA1
10	0*	0*	0*	1**	1**	0	0	0C	1	0	0	Y SA1
11	1	1	1	1**	1**	0	0	7C	0*	0*	0	F+Z SA1
12	1	1	1	1**	1**	1	1	7F	0*	0*	0	F SA0
13	0*	0*	0*	0	0	0	1	01	1	1	1	Z SA0

Full test vector table is created from methods carried out from theory

Table 2: Initial Truth Table

Key for tables:

* One condition must be set to logic 0

** One condition must set to logic 1

Good identification of key rule for redundancy

The tests from Table 2 show duplicates in tests 1 and 9, in 5, 8 and 13. As only one test is needed, redundancies can be made to reduce the number of tests. The test vectors after redundancies were applied are shown in Table 3.

Test No	A	B	C	D	E	F	Qgood	HEX	X	Y	Z	Fault
1	1	1	1	0	0	0	0	70	0	1	0	A+B+C SA0, X SA1
2	0	1	1	0	0	0	1	31	1	1	1	A SA1
3	1	0	1	0	0	0	1	51	1	1	1	B SA1
4	1	1	0	0	0	0	1	61	1	1	1	C SA1
5	0*	0*	0*	0	0	0	1	01	1	1	1	D+E SA1, X+Y SA0, Z SA0
6	0*	0*	0*	1	0	0	0	08	1	0	0	D SA0
7	0*	0*	0*	0	1	0	0	04	1	0	0	E SA0
10	0*	0*	0*	1**	1**	0	0	0C	1	0	0	Y SA1
11	1	1	1	1**	1**	0	0	7C	0*	0*	0	F+Z SA1
12	1	1	1	1**	1**	1	1	7F	0*	0*	0	F SA0

Redundancy identified and removed according to wildcard rule

Table 3: Reduced truth table using redundancy

The amount of test from Table 3 can be further reduced because of the wildcard equivalence rule, these test vectors are found with '*' and '**' in the table. Due to this rule, test 5 could be manipulated to become the same as test 4 as only one-off A, B, or C needs to be at logic 0. Once they are the same, it becomes a redundant test vector and can be removed like the first reduction. Test 6 and 10 can have the same rule applied. This now reduces the number of test vectors down to 8 from the original 13 in Table 2.

Good explanation of redundancy methods used to further reduce number of test vectors

The final test vectors are shown in Table 4 below.

Test No	A	B	C	D	E	F	Qgood	HEX	X	Y	Z	Fault
1	1	1	1	0	0	0	0	70	0	1	0	A+B+C SA0, X SA1
2	0	1	1	0	0	0	1	31	1	1	1	A SA1
3	1	0	1	0	0	0	1	51	1	1	1	B SA1
4	1	1	0	0	0	0	1	61	1	1	1	C SA1, D+E SA1, X+Y SA0, Z SA0
6	0*	0*	0*	1	0	0	0	08	1	0	0	D SA0, Y SA1
7	0*	0*	0*	0	1	0	0	04	1	0	0	E SA0
11	1	1	1	1**	1**	0	0	7C	0*	0*	0	F+Z SA1
12	1	1	1	1**	1**	1	1	7F	0*	0*	0	F SA0

Table 4: Final Test Vector Table

3.3 MultiSim Design Tests using Word Generator

A word generator was used on MultiSim to test the circuit under test with no-fault condition. The circuit is shown in Figure 13.

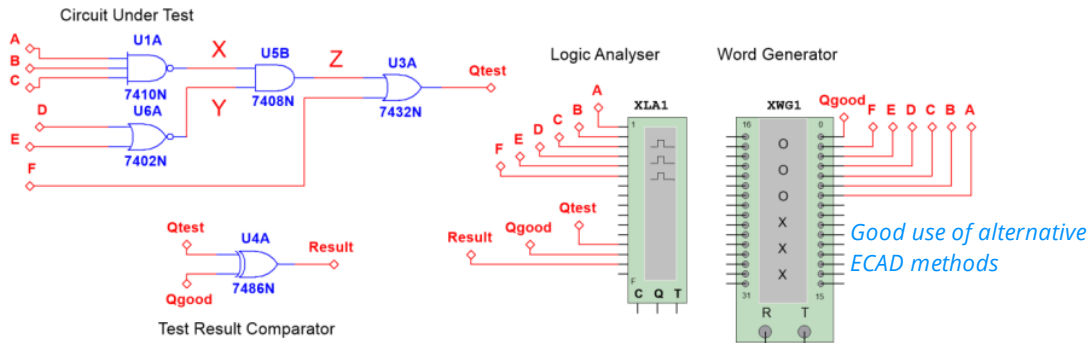


Figure 13: MultiSim simulation - No fault Condition

Figure 14 shows the waveform from the logic analyser. The trace of the analyser shows a constant at logic 0 proving the XOR output is at 0 in the highlighted box when the circuit was under test.

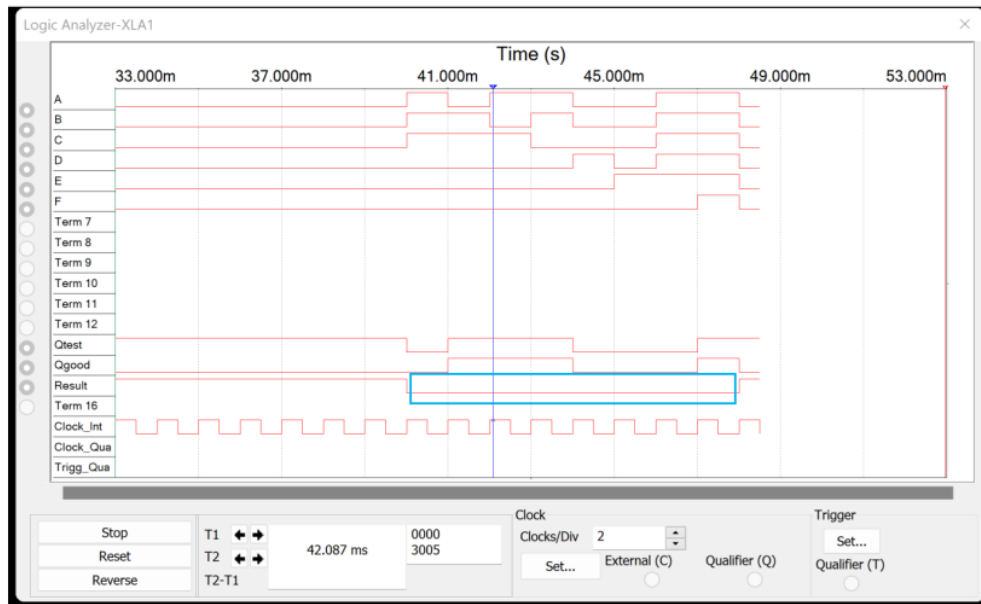


Figure 14: Logic Analyser No Fault Condition

Good explanation and illustrated example of NFF condition

4. Analysis of NI MultiSim results

4.1 Circuit Under Test

The circuit under test was then tested on MultiSim with three different faults on the circuit with fault condition set by the truth table of test vectors.

Input B stuck at logic 0

Figure 15 shows the circuit under test with input B stuck at 0.

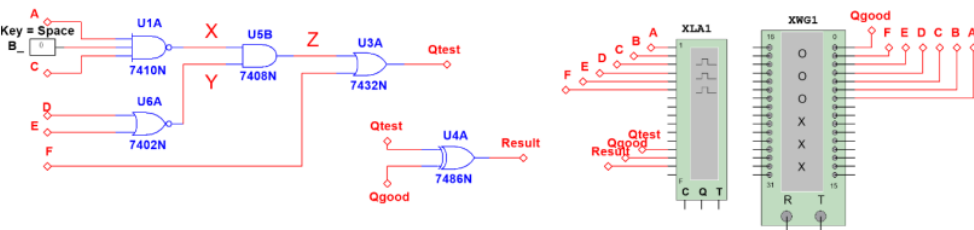


Figure 15: Input B SA0

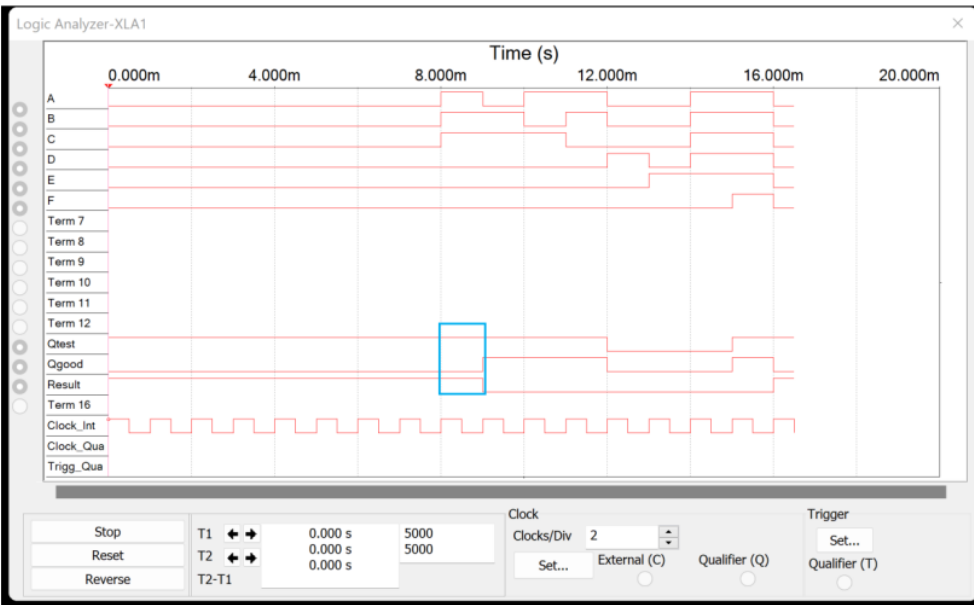


Figure 16: Input B SA0 analyser

Good illustration of fault condition and results

Figure 16 shows the trace from the logic analyser. The high output in the 'result' from the X-OR gate shows there is a fault on the circuit. The 'Qtest' and 'Qgood' outputs should be the same when the circuit is not in fault condition.

Input B Stuck at logic 1

Figure 17 shows input B stuck at logic 1. Figure 18 shows the logic analyser for this fault. The blue highlights the fault condition where 'Result' goes to logic 1.

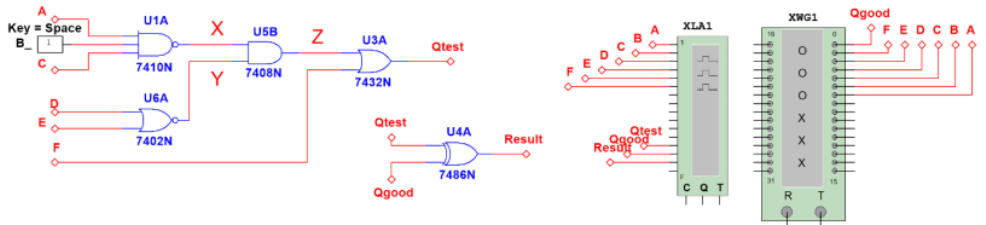


Figure 17: Input B SA1

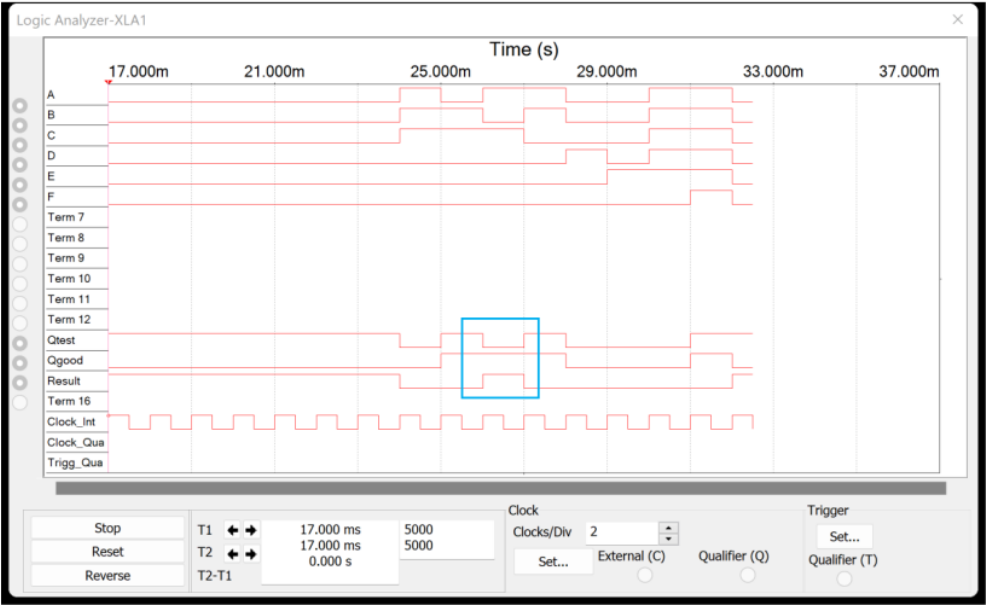


Figure 18: Input B SA1 analyser

Good test result

Input D stuck at logic 0

Figure 19 shows input D stuck at logic 0.

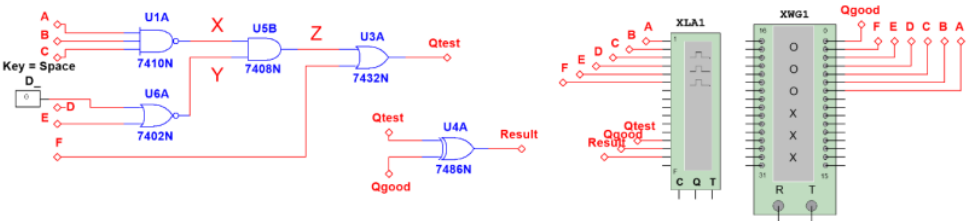
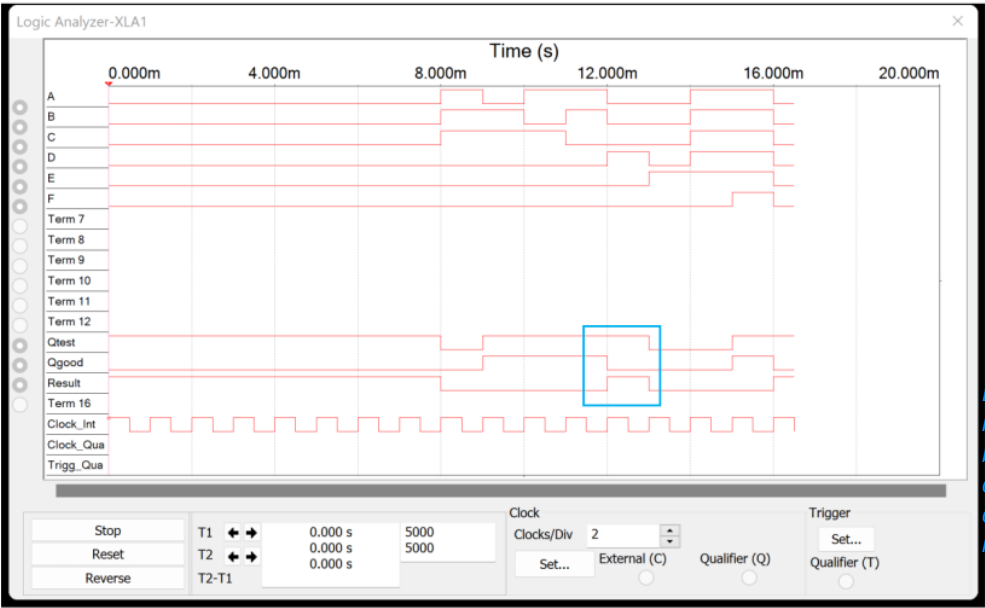


Figure 19: Input D SA0



ECAD test results have been explained and appropriately illustrated

Figure 20: Input D SA0 analyser

Figure 20 shows the logic analyser when input D is stuck at zero. As with the previous fault conditions, the result trace goes positive, representing a fault on the circuit.

4.2 6-Bit Register

A 6-bit register ATE test was designed and implemented for the circuit under test. The same fault conditions were used for fault testing and analysis. Table 5 shows the next state condition for the finite state machine for test vectors A to F.

PRESENT STATE						NEXT STATE					
A	B	C	D	E	F	A+	B+	C+	D+	E+	F+
1	1	1	0	0	0	0	1	1	0	0	0
0	1	1	0	0	0	1	0	1	0	0	0
1	0	1	0	0	0	1	1	0	0	0	0
1	1	0	0	0	0	0	0	0	1	0	0
0	0	0	1	0	0	0	0	0	0	1	0
0	0	0	0	1	0	1	1	1	1	1	0
1	1	1	1	1	0	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	0	0	0

Table 5: Next State Table

The table works by showing the binary code of the current state and the next state shows the binary code of the next state of the machine. This is verified by checking the next line of the present state table as highlighted below in Table 6.

PRESENT STATE						NEXT STATE					
A	B	C	D	E	F	A+	B+	C+	D+	E+	F+
1	1	1	0	0	0	0	1	1	0	0	0
0	1	1	0	0	0	1	0	1	0	0	0
1	0	1	0	0	0	1	1	0	0	0	0
1	1	0	0	0	0	0	0	0	1	0	0
0	0	0	1	0	0	0	0	0	0	1	0
0	0	0	0	1	0	1	1	1	1	1	0
1	1	1	1	1	0	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	0	0	0

Table 6: Next State Table Explanation

Good explanation of next state

Using the state tables, Karnaugh maps were utilised to generate the required logic states for the combinational logic for the input sequence. Table 7 shows the Boolean expressions from the Karnaugh maps.

Output	Boolean Expression	Map – Appendix A
QA	$A.B.C.D.E + A.NB.C.ND.NE.NF + NA.B.C.ND.NE.NF + NA.NB.NC.ND.E.NF$	Figure 37
QB	$A.C.ND.NE.NF + A.B.C.D.E + NA.NB.NC.ND.E.NF$	Figure 38
QC	$NA.NB.NC.ND.E.NF + NA.B.C.ND.NE.NF + A.B.C.ND.NE.NF + A.B.C.D.E$	Figure 39
QD	$NA.NB.NC.ND.E.NF + A.B.NC.ND.NE.NF + A.B.C.D.E.NF$	Figure 40
QE	$NA.NB.NC.ND.E.NF + NA.NB.NC.D.NE.NF + A.B.C.D.E.NF$	Figure 41
QF	$A.B.C.D.E.NF$	Figure 42

Table 7: Karnaugh Map Boolean Expressions

Figure 21 below shows the 6-bit register with combination feedback circuit with no fault condition being created from the Boolean expressions from the Karnaugh maps. The circuit under test result is then compared against the output of a known working circuit with an X-OR gate used as a comparator to identify when the circuit has a fault.

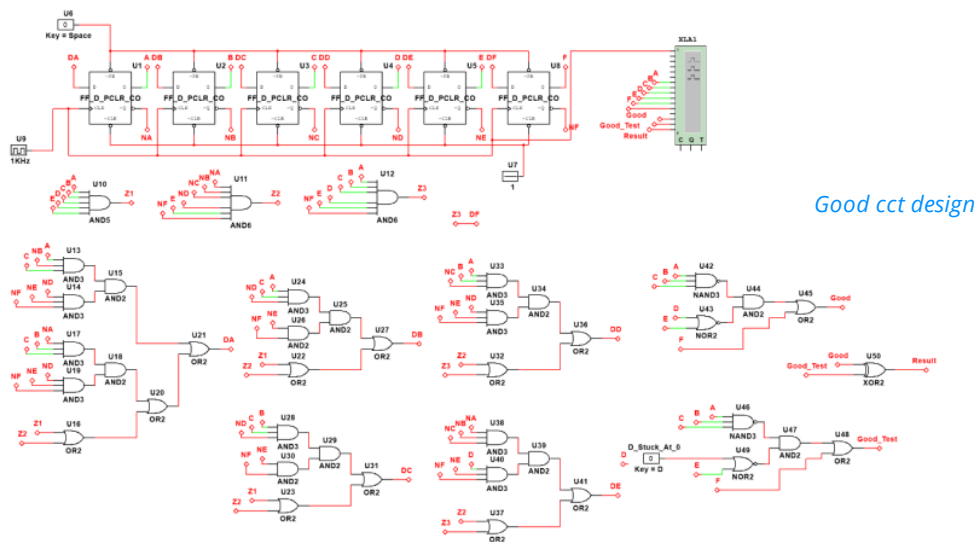
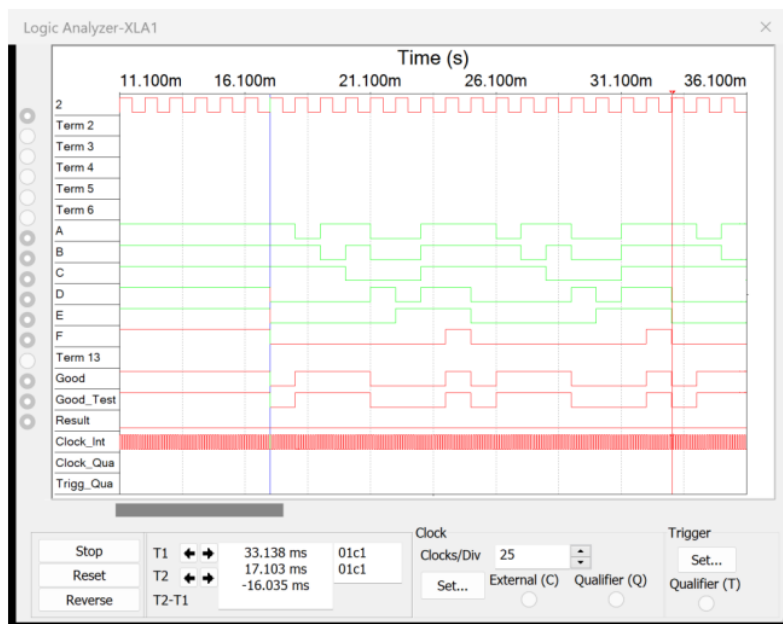


Figure 21: 6-Bit register with no fault condition



NFF condition is determined. This is a significant stage to achieve before any tests can be carried out

Figure 22: 6-BIT generator no fault condition

Figure 22 shows the trace from the logic analyser for the circuit with no fault condition between the two cursors and proves there is no fault as the 'Result' stays at logic 0.

The same faults were replicated again with input stuck at logic 0, then at logic 1 concluding with input D stuck at logic 0.

Figure 23 and Figure 24 shows the circuit and logic analyser for input B stuck at 0. The fault has been highlighted and can be seen when the result pulses to logic 1.

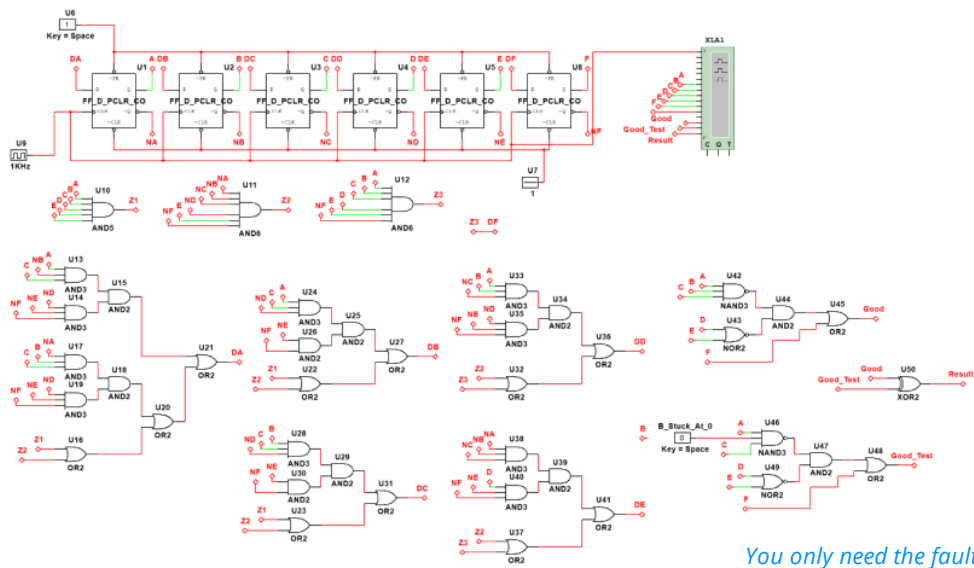


Figure 23: Input B SA0

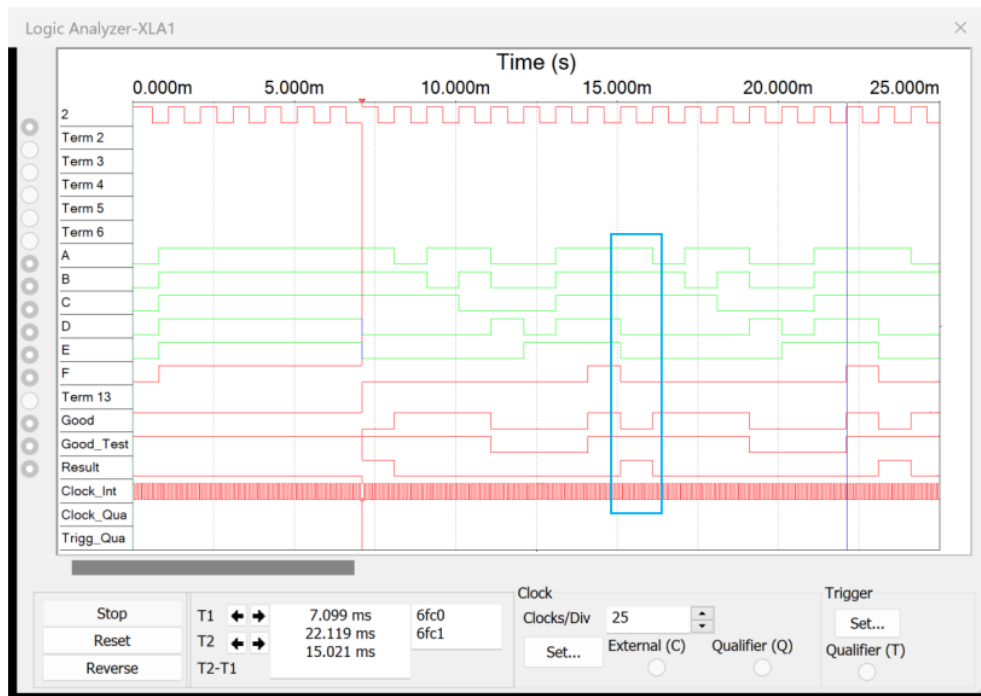


Figure 24: Input B SA0 Fault

Fault is clearly identified

Figure 27 shows the circuit for when input D in SA0 and Figure 28 shows the logic analyser with the fault highlighted when result goes to logic 1.

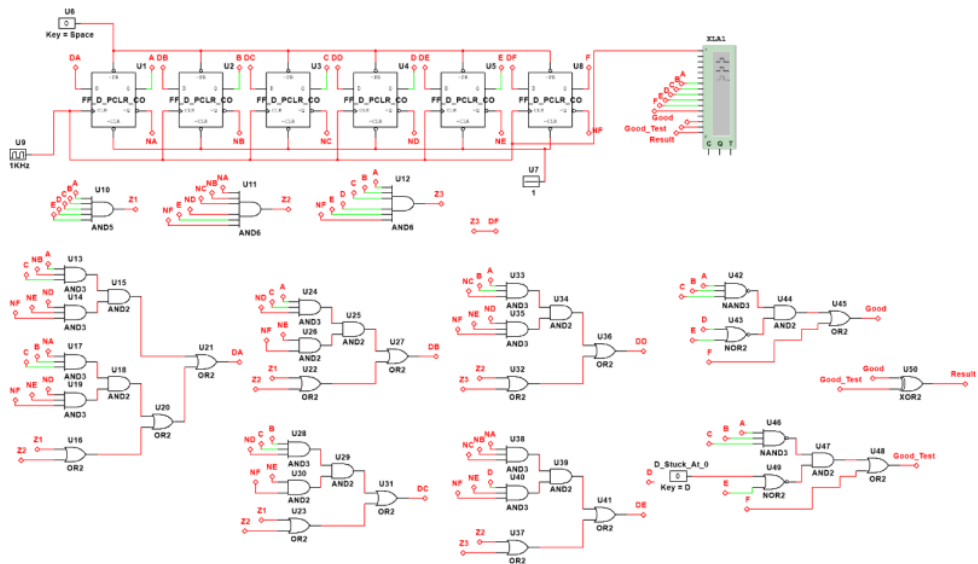


Figure 27: Input D SA0

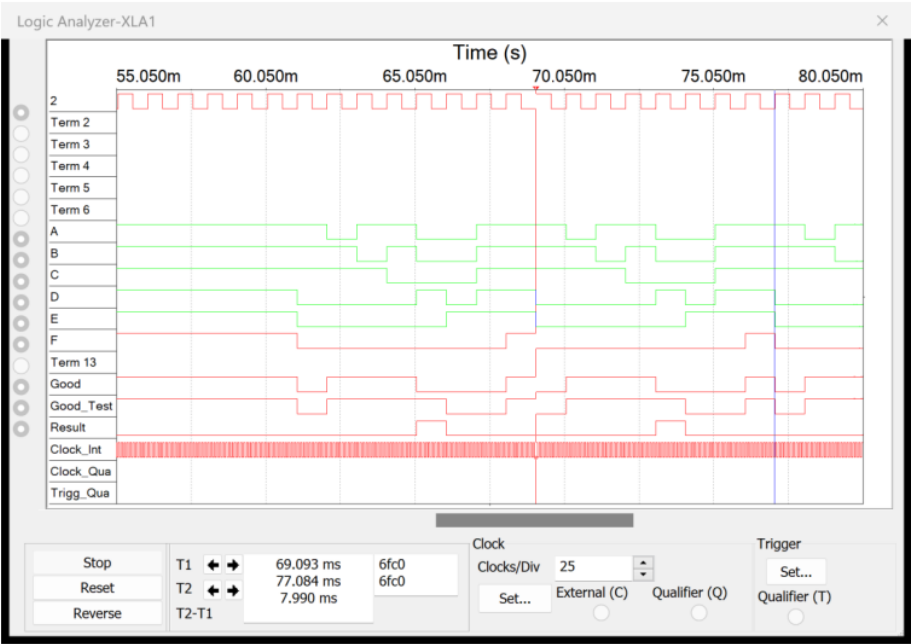


Figure 28: Input D SA0 Fault

Faults are identified and explained

5. Practical build and test using Labview

NI Labview was also used to test the identical CUT. A NI Elvis II DAQ development board was used to provide the interface and the associated interfaced library was added as a plugin option on NI Labview. The block diagram and G code in NI Labview which supplies the control for the CUT inputs is shown below in Figure 29

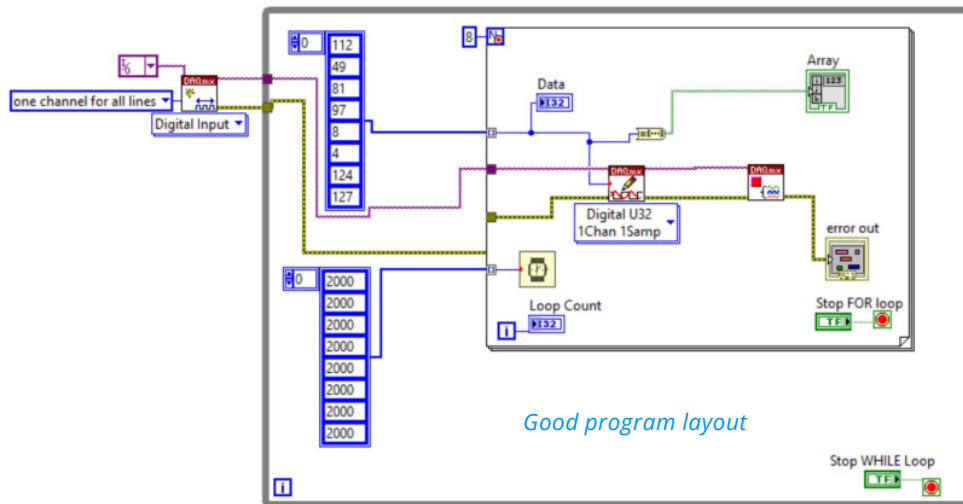


Figure 29: CUT input driver via DAQ Outputs

The result from the CUT then feeds back into NI Labview via the DAQ inputs to display data on the Labview interface. The block diagram is shown in Figure 30.

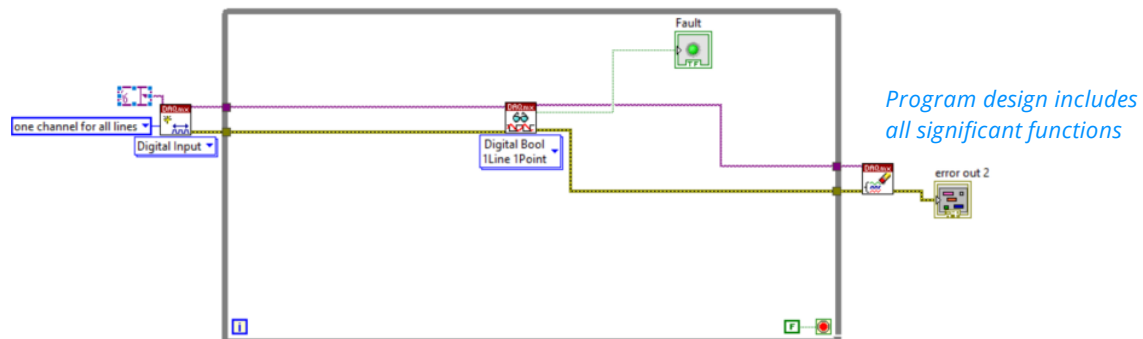


Figure 30: X-OR Gate comparator via DAQ Inputs

The board was subsequently tested under no-fault condition as shown in Figure 31 and Figure 32.

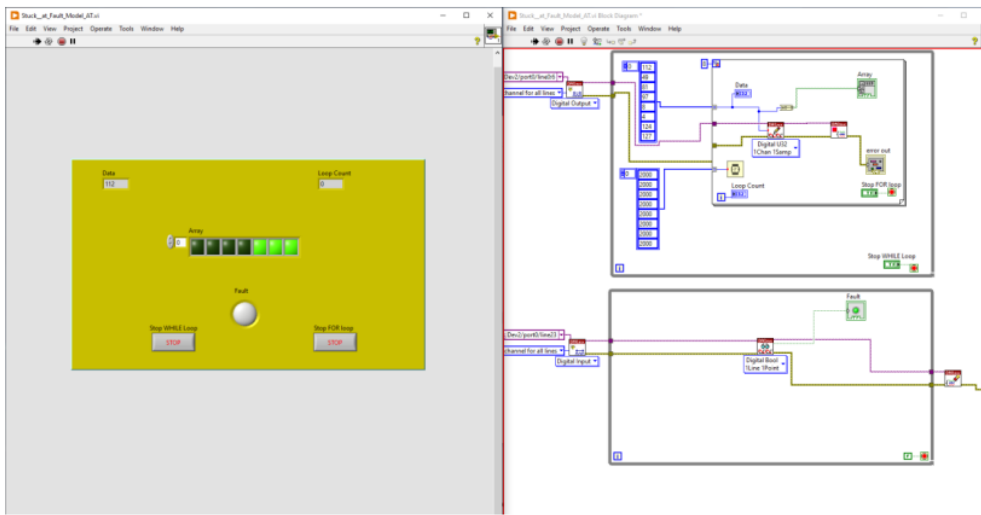


Figure 31: NI Labview no fault condition

Program is tested under NFF condition with good test example

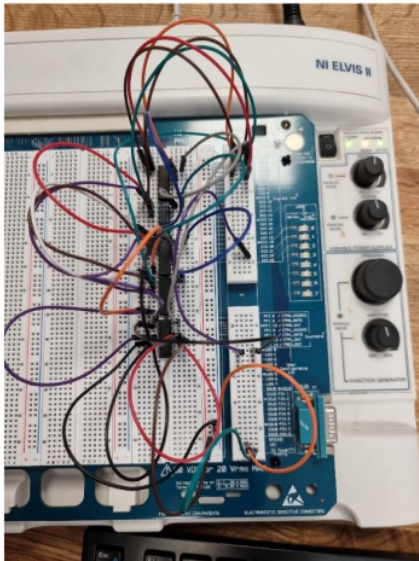


Figure 32: NI Elvis II DAQ development board no fault condition

The same three test faults used in the MultiSim test were applied to the DAQ board. Table 8 summarises the faults used in this test.

Fault Condition	NI Labview	DAX board
Input B SA0	Appendix B - Figure 43	Appendix B - Figure 44
Input B SA1	Appendix B - Figure 45	Appendix B - Figure 46
Input D SA0	Appendix B - Figure 47	Appendix B - Figure 48

Table 8: NI Labview 3 Fault conditions

Good use of table with ref to appendix

The PCB board was then connected to the Elvis DAQ board and tested using the same fault conditions. The PCB with no-fault condition is shown in Figure 33 and Figure 34.

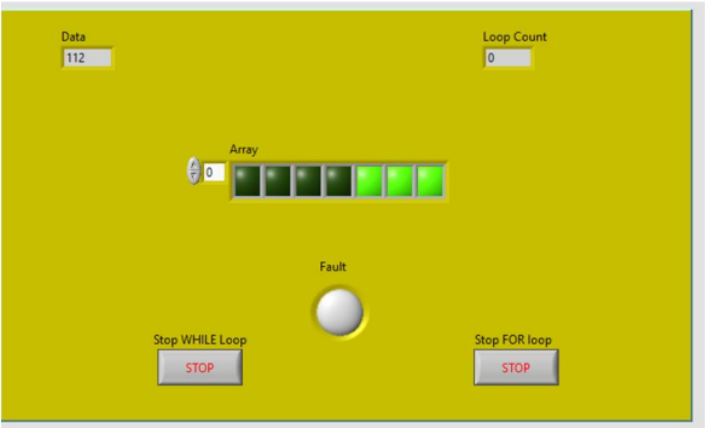
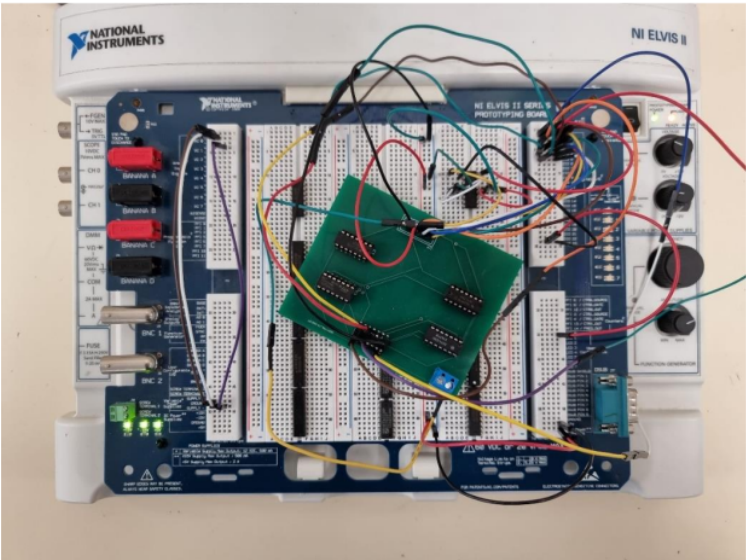


Figure 33: Labview with PCB - no fault condition



NFF is identified

Figure 34: PCB under test using LabVIEW and Elvis DAQ – no fault condition

Table 9 shows the fault conditions for the PCB.

Fault Condition	NI Labview	DAX board & PCB
Input B SA0	Appendix C - Figure 49	Appendix C - Figure 50
Input B SA1	Appendix C - Figure 51	Appendix C - Figure 52
Input D SA0	Appendix C - Figure 53	Appendix C - Figure 54

Table 9: PCB test conditions

Good use of table with ref to appendix

6. CAM Design and Build of Prototype

The test circuit was then built on CAM (Computer-aided manufacturing) software called Eagle. Once built, the resulting Gerber files could be sent to a manufacturer to produce the PCB board with the built-in circuit. Figure 35 shows the schematic and Figure 36 shows the design for the PCB board in the Eagle software. The Gerber files are presented in Appendix D Figure 55 to Figure 60.

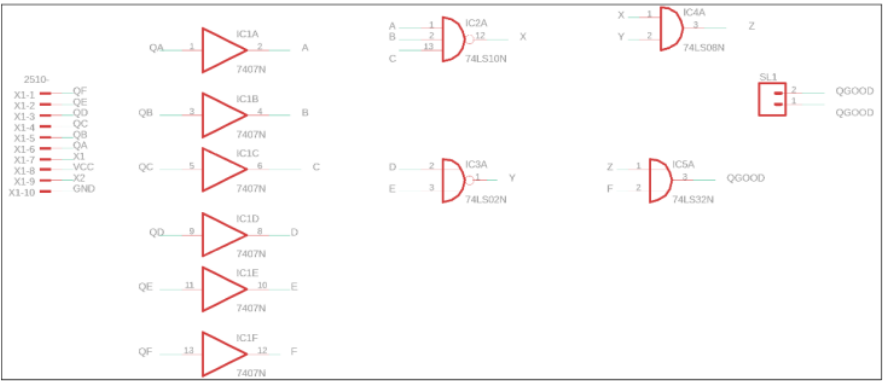


Figure 35: Eagle CAD Schematic

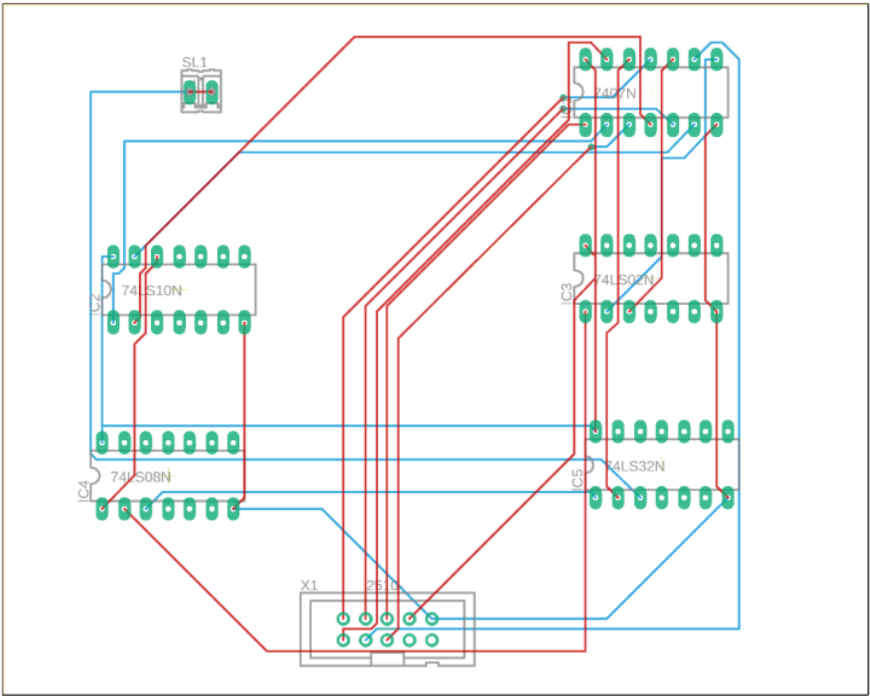


Figure 36: Board design in Eagle

Good CAM schematic and PCB design

7. Conclusions and Recommendations

Following analysis of the ATE designs and results to demonstrate that the prototype met customer needs, it was concluded that the circuit under test met the design requirement of a 6-input combinational circuit. The number of test vectors was successfully reduced using the stuck-at-model from 13 tests down to 8. The test vectors were able to be reduced as tables were used to quantify the redundant tests by identifying duplicate results and further reduction through the wildcard method which allowed for alteration of select inputs.

Using a word generator in MultiSim, inputs could be generated for the CUT using the test vectors. A no-fault condition test was first carried out to prove the CUT was operating correctly and is fault-free to start. Three tests from the resultant tables were conducted on the circuit, input B SA 0, input B SA1 and input D SA0. The circuit was tested and the output was compared through a X-OR gate against a good result to find any faults on the CUT.

A 6-bit pattern generator ATE system with the CUT under the same conditions was constructed and the tests were repeated, with all tests successfully identifying their faults proving the prototype.

G-code and the block diagrams were created on NI Labview, and the circuit tested using the same test faults with the DAQ interface board. This test highlighted the need to always start with testing no-fault condition as the fault-indicator showed a fault on the first test. This led to a review of the block diagram and found an error with a block set to digital input not the required digital output. After the error was corrected, the remaining tests were successful and faults identified as expected, hence matching the theory to practical results.

The advantage of using Vision software such as Labview is it has the capability to use a graphical user interface (GUI) to process the data in real time giving a visual display to the user.

If this prototype was then to be sent to mass production several of the tests could be compiled together to ensure a fast-testing process and achieve reliable results. The Gerber files would be used as the board design for production where the operator would need to take suitable measures as identified in the research such as earth bonding and antistatic tools to prevent Electro Static Discharge. During testing, the machine vision process could detect any missing chips and wrong orientation, the bed-of-nails can then rapidly test the circuit through an automated process and a display result on a GUI such as Labview. Combining the test in an automated process would save a company a lot of money with less labour costs and removing the human error out of the process.

Good conclusion and relevant recommendation

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Extensive reference sources listed

9. Appendix

9.1 Appendix A – Karnaugh Maps

ABC/DEF	000	001	011	010	100	101	111	110
000	0	0	1	0	0	1	0	0
001	0	0	0	0	0	0	0	0
011	0	0	0	0	0	0	0	0
010	1	0	0	0	0	0	0	0
100	0	0	0	0	0	0	0	0
101	0	0	0	0	0	0	0	0
111	0	0	0	0	0	0	1	0
110	0	0	0	0	0	0	1	0

Figure 37: Karnaugh Map - QA

ABC/DEF	000	001	011	010	100	101	111	110
000	0	0	0	0	0	1	1	0
001	0	0	0	0	0	0	0	0
011	0	0	0	0	0	0	0	0
010	1	0	0	0	0	0	0	0
100	0	0	0	0	0	0	0	0
101	0	0	0	0	0	0	0	0
111	0	0	0	0	0	0	1	0
110	0	0	0	0	0	0	1	0

Figure 38: Karnaugh Map - QB

ABC/DEF	000	001	011	010	100	101	111	110
000	0	0	1	0	0	0	1	0
001	0	0	0	0	0	0	0	0
011	0	0	0	0	0	0	0	0
010	1	0	0	0	0	0	0	0
100	0	0	0	0	0	0	0	0
101	0	0	0	0	0	0	0	0
111	0	0	0	0	0	0	1	0
110	0	0	0	0	0	0	1	0

Figure 39: Karnaugh Map - QC

ABC/DEF	000	001	011	010	100	101	111	110
000	0	0	0	0	0	0	0	1
001	0	0	0	0	0	0	0	0
011	0	0	0	0	0	0	0	0
010	1	0	0	0	0	0	0	0
100	0	0	0	0	0	0	0	0
101	0	0	0	0	0	0	0	0
111	0	0	0	0	0	0	0	0
110	0	0	0	0	0	0	1	0

Figure 40: Karnaugh Map - QD

ABC/DEF	000	001	011	010	100	101	111	110
000	0	0	0	0	0	0	0	0
001	0	0	0	0	0	0	0	0
011	0	0	0	0	0	0	0	0
010	1	0	0	0	0	0	0	0
100	1	0	0	0	0	0	0	0
101	0	0	0	0	0	0	0	0
111	0	0	0	0	0	0	0	0
110	0	0	0	0	0	0	1	0

Not a group due to 6 variable K-MAP rules

Figure 41: Karnaugh Map - QE

ABC/DEF	000	001	011	010	100	101	111	110
000	0	0	0	0	0	0	0	0
001	0	0	0	0	0	0	0	0
011	0	0	0	0	0	0	0	0
010	0	0	0	0	0	0	0	0
100	0	0	0	0	0	0	0	0
101	0	0	0	0	0	0	0	0
111	0	0	0	0	0	0	0	0
110	0	0	0	0	0	0	1	0

Figure 42: Karnaugh Map - QF

Good use of appendix

9.2 Appendix B – NI Labview and DAQ Board

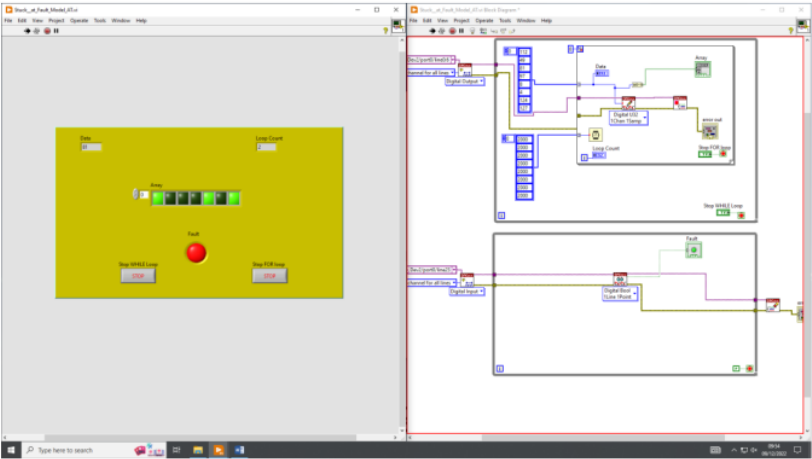


Figure 43: NI Labview B SA0

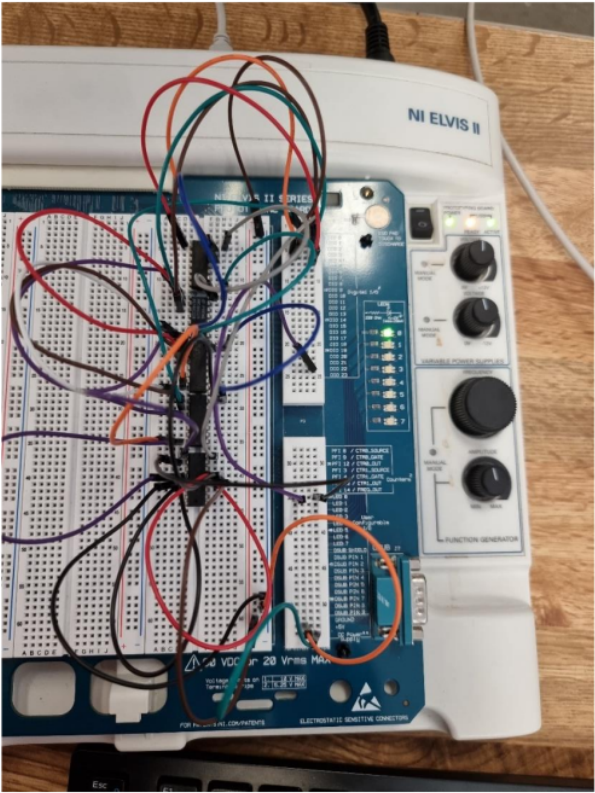


Figure 44: NI Elvis II DAQ development board B SA0

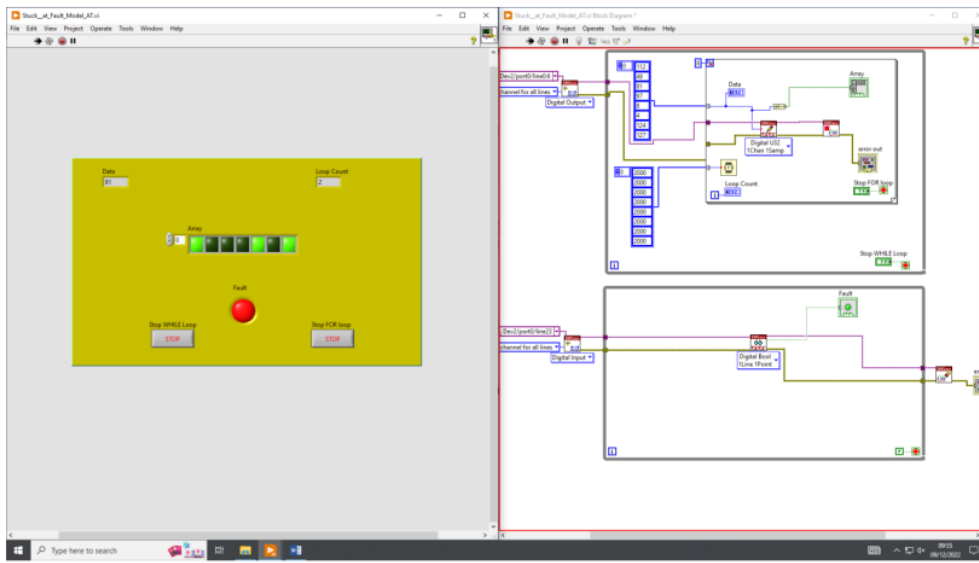


Figure 45: NI Labview B SA1

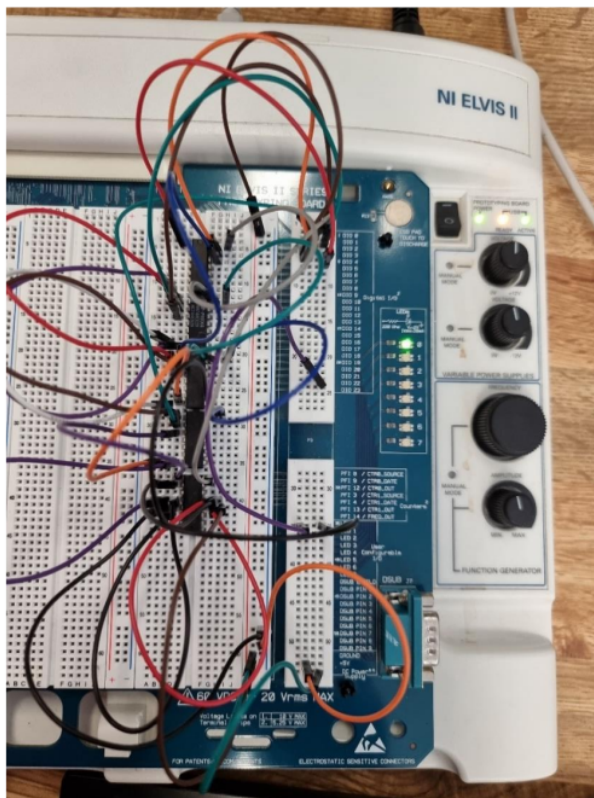


Figure 46: NI Elvis II DAQ development board B SA1

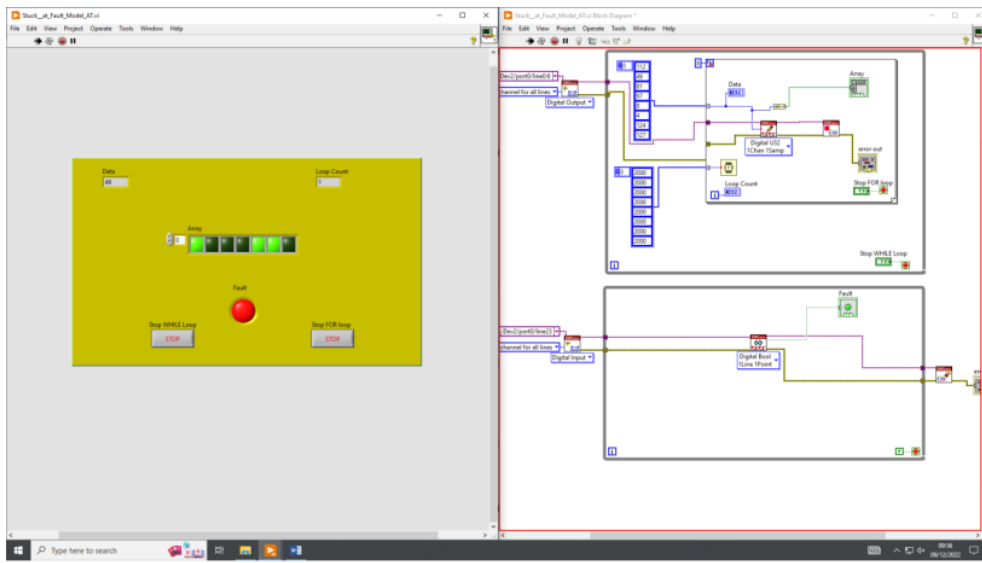


Figure 47: NI Labview D SA0

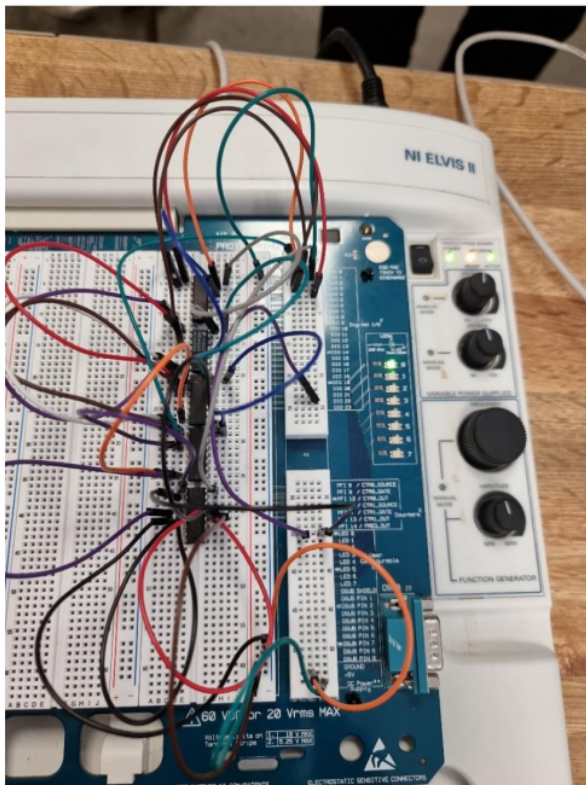


Figure 48: NI Elvis II DAQ development board D SA0

Fault conditions are tested and result is returned to LabVIEW

9.3 Appendix C – NI Labview with PCB via DAQ Board

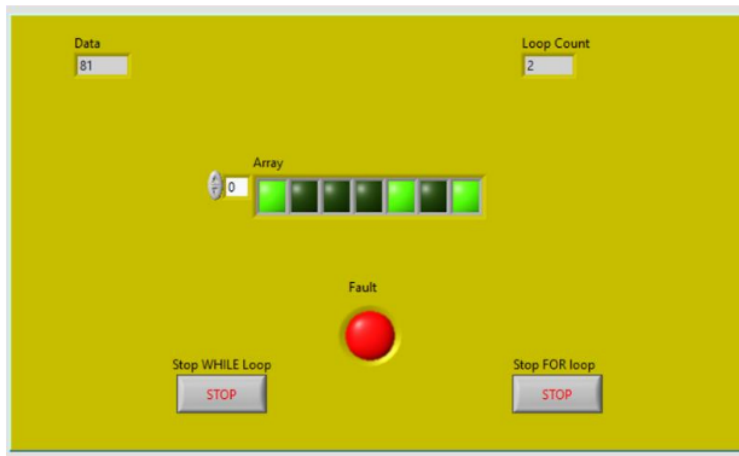


Figure 49: NI Labview with PCB input B SA0

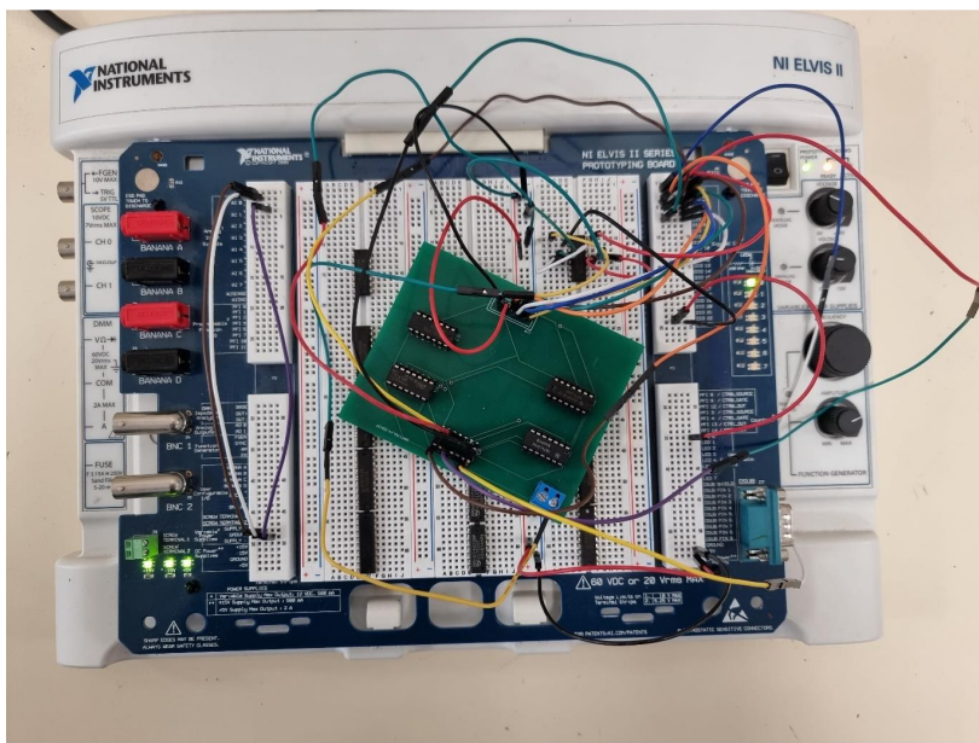


Figure 50: PCB under test using LabVIEW and Elvis DAQ – Input B SA0

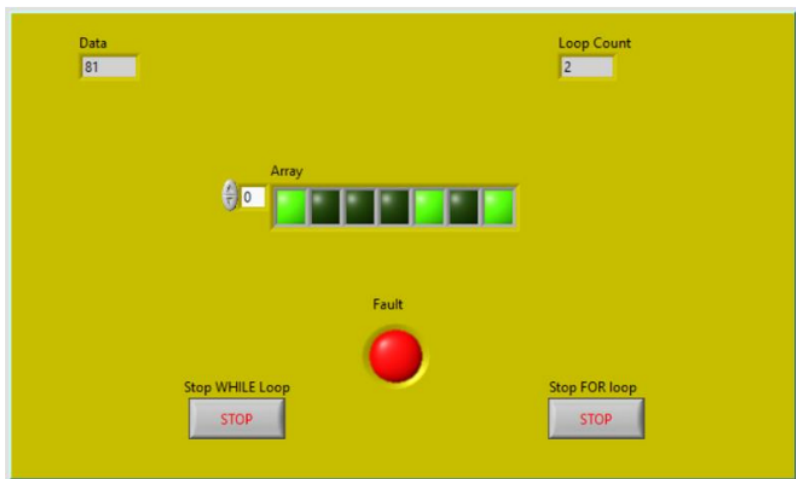


Figure 51: NI Labview with PCB input B SA1

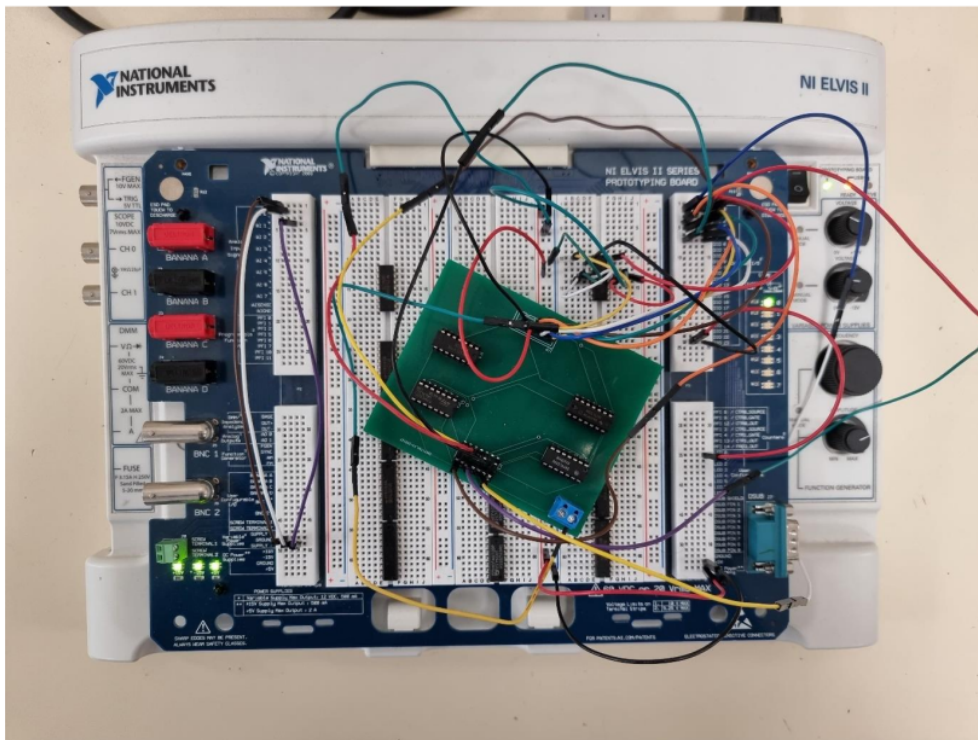


Figure 52: PCB under test using LabVIEW and Elvis DAQ – Input B SA1

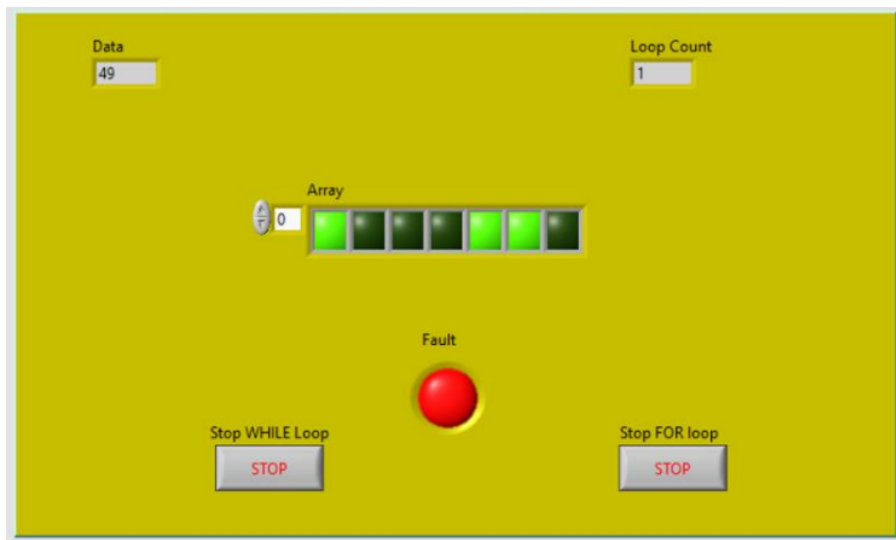


Figure 53: NI Labview with PCB input D SA0

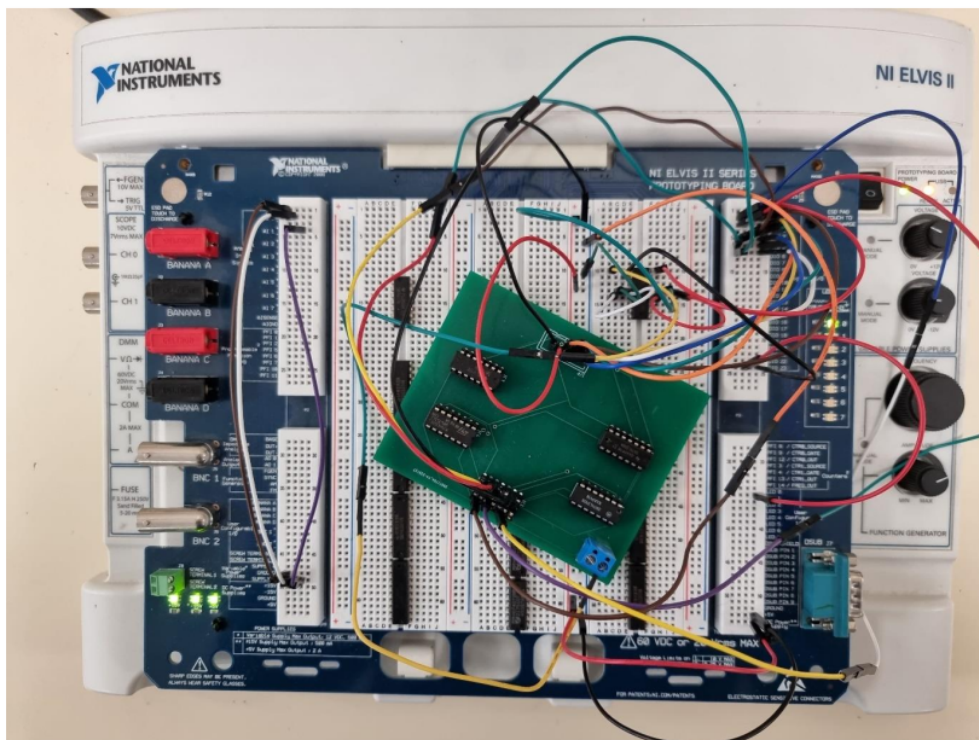


Figure 54: PCB under test using LabVIEW and Elvis DAQ – Input D SA0

PCB testing is correct with good results indicated

9.4 Appendix D – Gerber Files

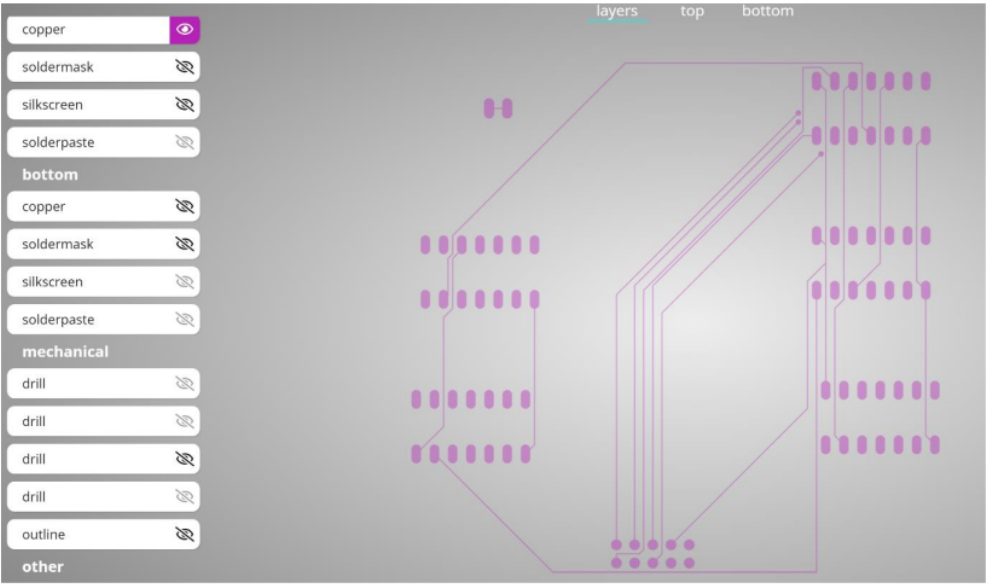


Figure 55: Gerber File Top Layer – Copper

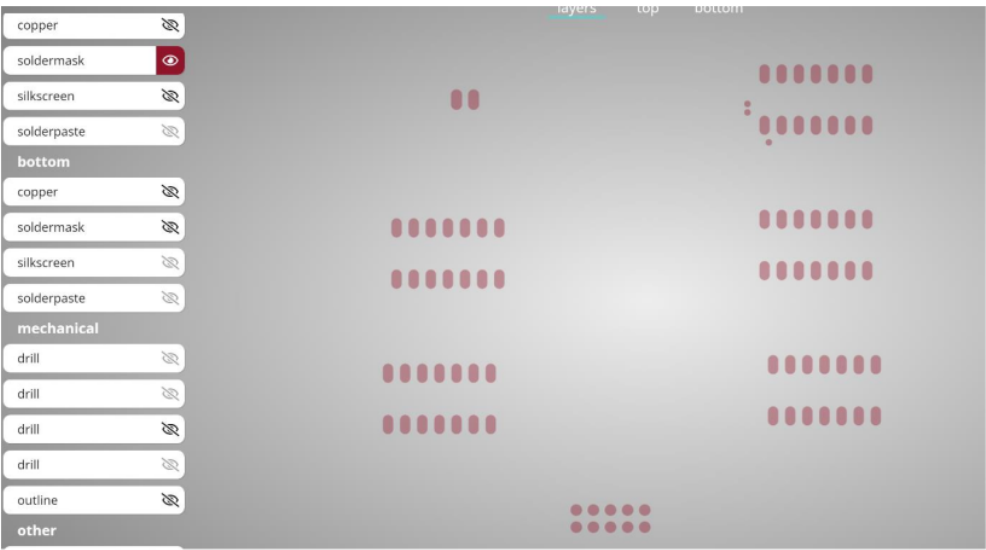


Figure 56: Gerber File Top Layer – Soldermask

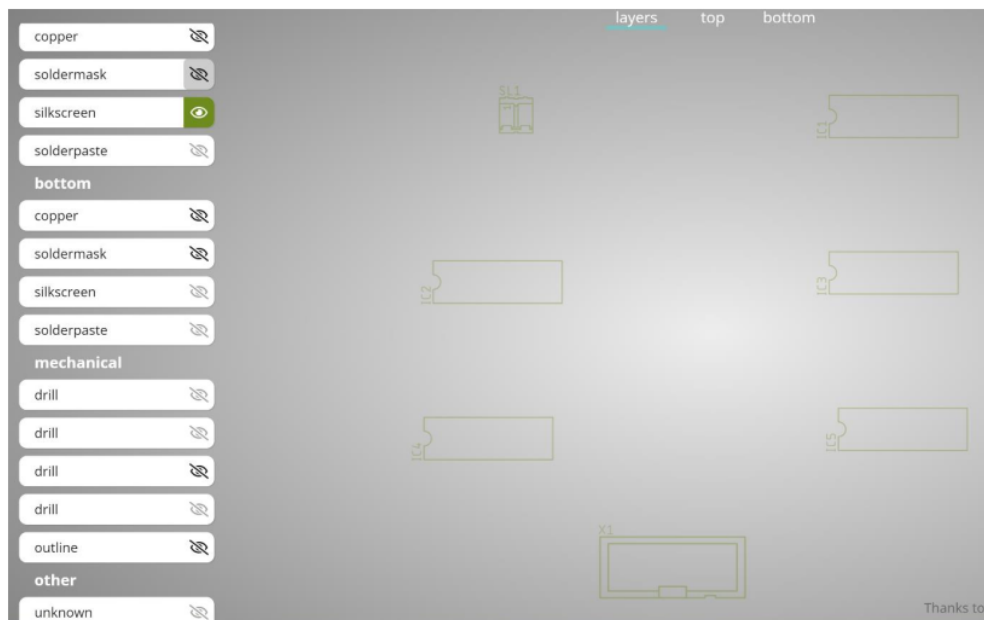


Figure 57: Gerber File Top Layer – Silkscreen

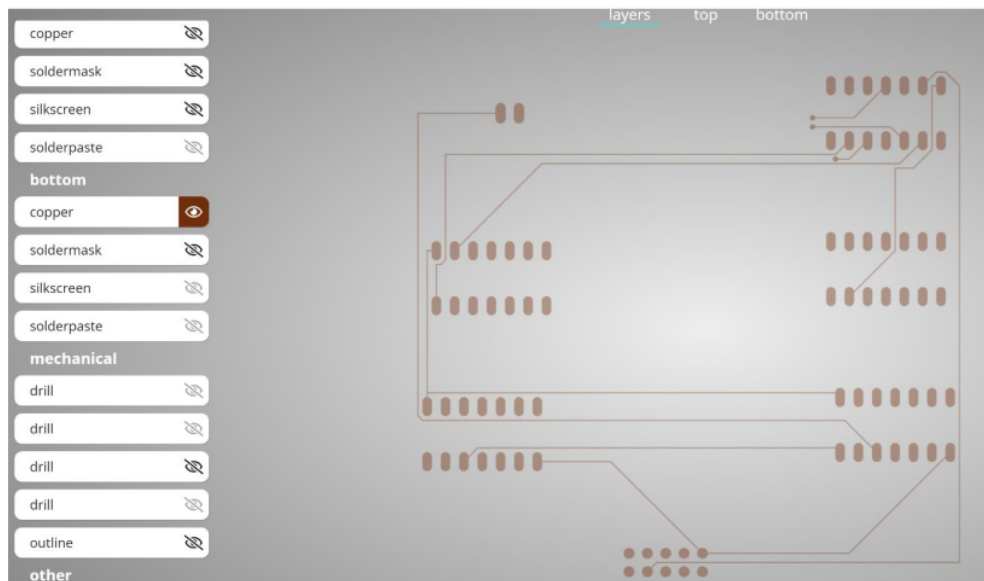


Figure 58: Gerber File Bottom Layer – Copper

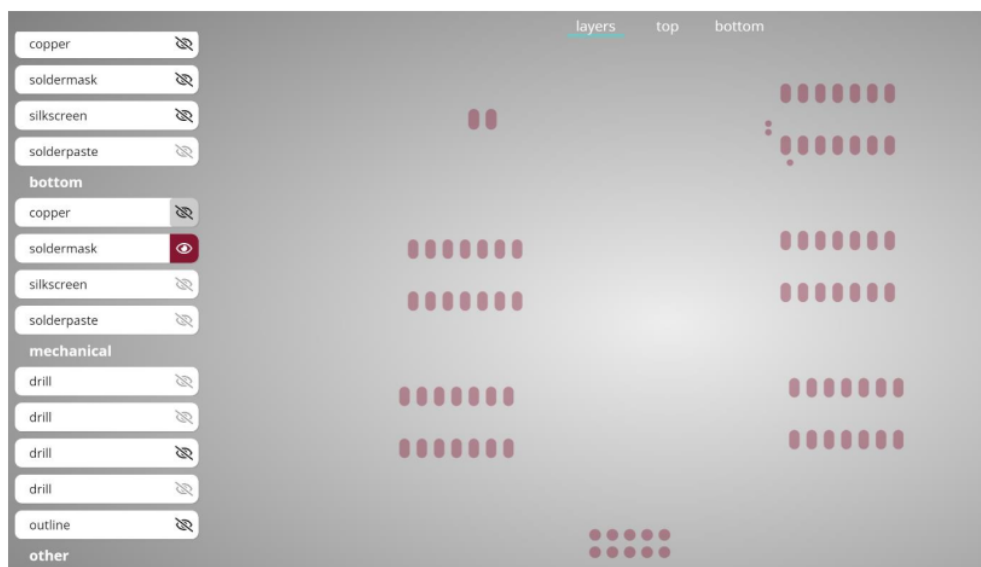


Figure 59: Gerber File Bottom Layer – Soldermask

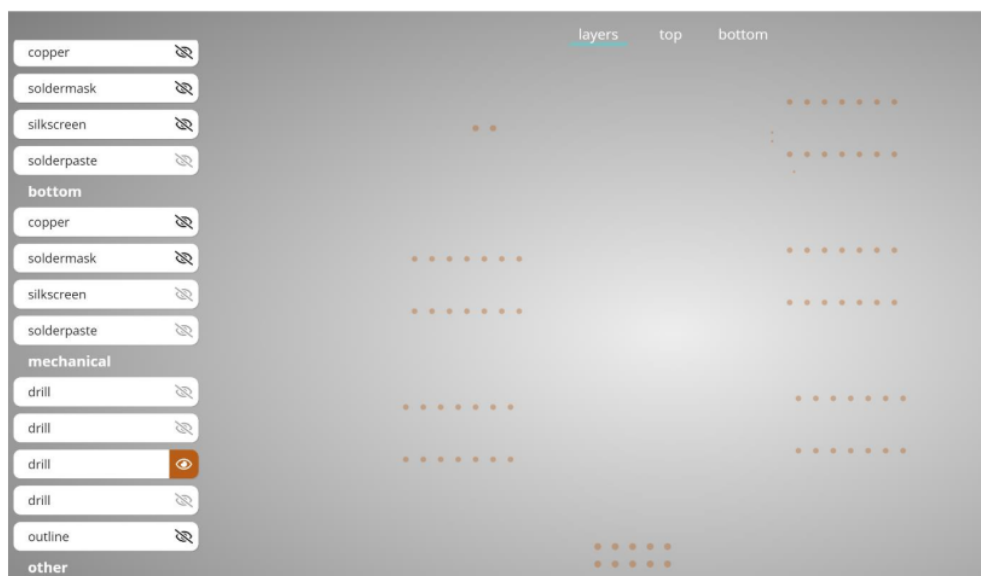


Figure 60: Gerber File Mechanical Layer - Drill holes

Gerber files needed for production have been identified

1909751

GRADEMARK REPORT

FINAL GRADE

GENERAL COMMENTS

Instructor

76/100

PAGE 1

PAGE 2

PAGE 3

Text Comment. Good detailed table of contents

PAGE 4

PAGE 5

Text Comment. Good extensive list of figures

PAGE 6

Text Comment. Good list of tables

PAGE 7

Text Comment. Summary demonstrates a good understanding of the requirements and purpose of the tasks

PAGE 8

Text Comment. Good explanation with examples

PAGE 9

Text Comment. Good research carried out on this topic

Text Comment. Good explanation with relevant example

Text Comment. Good research carried out

Text Comment. An industrial application example should be used here

Text Comment. Good coverage on this with relevant points made

Text Comment. Good explanation and example

Text Comment. Relevant preventive measures are covered and explained in good detail, with application example

Text Comment. SSF reduction methods carried out for each gate and explained using examples

Text Comment. Full test vector table is created from methods carried out from theory

Text Comment. Good identification of key rule for redundancy

Text Comment. Redundancy identified and removed according to wildcard rule

Text Comment. Good explanation of redundancy methods used to further reduce number of test vectors

Text Comment. Good use of alternative ECAD methods

Text Comment. Good explanation and illustrated example of NFF condition

Text Comment. Good illustration of fault condition and results

Text Comment. Good test result

Text Comment. ECAD test results have been explained and appropriately illustrated

Text Comment. Good explanation of next state

Text Comment. Good use of table and ref to appendix figures

Text Comment. Good cct design

Text Comment. NFF condition is determined. This is a significant stage to achieve before any tests can be carried out

Text Comment. You only need the fault condition here!

Text Comment. Fault is clearly identified

Text Comment. Fault is clearly identified

Text Comment. Faults are identified and explained

Text Comment. Good program layout

Text Comment. Program design includes all significant functions

PAGE 28

Text Comment. Program is tested under NFF condition with good test example

Text Comment. Good use of table with ref to appendix

PAGE 29

Text Comment. NFF is identified

Text Comment. Good use of table with ref to appendix

PAGE 30

Text Comment. Good CAM schematic and PCB design

PAGE 31

Text Comment. Good conclusion and relevant recommendation

PAGE 32

PAGE 33

PAGE 34

Text Comment. Extensive reference sources listed

PAGE 35

PAGE 36

PAGE 37

Text Comment. Good use of appendix

PAGE 38

PAGE 39

PAGE 40

Text Comment. Fault conditions are tested and result is returned to LabVIEW

Text Comment. PCB testing is correct with good results indicated

Text Comment. Gerber files needed for production have been identified

GRADING FORM: CSG-RUBIC

ALEX WILLIAMS

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RESEARCH-INFORMED LITERATURE



Very good research carried out that covers significant relevant points for the topic area. The sources investigated demonstrates extensive research.

17/20

KNOWLEDGE AND UNDERSTANDING



A very good understanding in all areas and test vectors obtained using SSF rules. 4/5 LabVIEW design demonstrates a very high level of study during development. 4/5 ECAD alternative ATE

15/20

methods have been designed and developed using alternative functions to meet requirements. 4/5
CAM development demonstrates a good understanding. however, a more detailed explanation could have been included. 3/5

ANALYSIS

 Good ECAD analysis of test results that are supported with relevant evidence images. 8/10
Tests carried out follow the results derived from tables, and thus from theory. 3.5/5 Good conclusion and a valid recommendation included. 3.5/5

15/20

PRACTICAL APPLICATION AND DEP.

 Good procedures used in the development and test of prototype with explanations. 7/10 Tests using LabVIEW method has been carried out with good illustrative evidence, with a good level of detail. 7/10

14/20

SKILLS FOR PROFESSIONAL PRAC.

 Extensive use of relevant software is evident and used effectively. 7.5/10 A good report with relevant word count for the content coverage, however slightly higher than allowable. 3.5/5 Report layout is good with all tasks in the correct order. Good table of contents and list of figures. 4/5

15/20