

LOCATION SWANSEA

LLEOLIAD ABERTAWE

LEVEL 5

LEFEL 5

**EXAMINATION PERIOD
MAY 2016**

**CYFNOD ARHOLIADAU
MAI 2016**

**MODULE CODE: M5X01118
DIGITAL ELECTRONICS**

TIME: 2 HOURS

ANSWER THREE QUESTION OUT OF FOUR

Equipment or materials required – None

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ANSWER THREE QUESTION OUT OF FOUR

1.

- a. A half adder circuit is described by the truth table of table Q1a1 and a full adder is described by the truth table of table Q1a2. Design circuits that are able to perform both of these functions.

<i>A</i>	<i>B</i>	<i>SUM</i>	<i>Cout</i>
0	0	0	0
0	1	1	0
1	0	1	0
1	1	1	1

Table Q1a1

<i>A</i>	<i>B</i>	<i>Cin</i>	<i>SUM</i>	<i>Cout</i>
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table Q1a2

(12 marks)

- b. Find a simplified expression for the function *F* represented by the map of figure Q3c.

CD \ AB				
	00	01	11	10
00	X	X	X	1
01	X	0	1	X
11	0	0	0	1
10	1	1	X	0

Figure Q3c

Note: 'X' signifies a 'Don't Care State'

(5 marks)

- c. Show, using block diagrams how half adders and full adders can be used to construct an 8-bit parallel adder.

(8 marks)

2.

- a. Design a circuit, using only NAND gates, that is able to implement the Boolean Algebra expression for P, as shown below.

$$P = A.B + A.C + B.C$$

(6 marks)

- b. Design a logic circuit that is able to display the numbers 0 to 7 on a seven segment display as shown in figure Q2b.

Note: Assume that a positive logic output switches on a display segment.

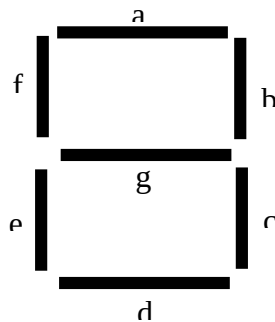


Figure Q2b

(19 marks)

3.

- a. Design a state diagram from the following specification:

The system must cycle through the count sequence $\dots, 0, 7, 6, 3, 4, 5, 0, 7, 6, 3, 4, 5, \dots$ continually while the input $HOLD = 1$. If $HOLD = 0$ then the system must remain in the current state. When $HOLD = 1$ then the above count sequence will once again commence.

NOTE: a circuit design is not required

(6 Marks)

- b. The figure Q4b represents a 2-bit adder circuit that is able to add two 2-bit numbers ($A = a_1a_0$ and $B = b_1b_0$) and produce a 3-bit result ($P = p_2p_1p_0$)

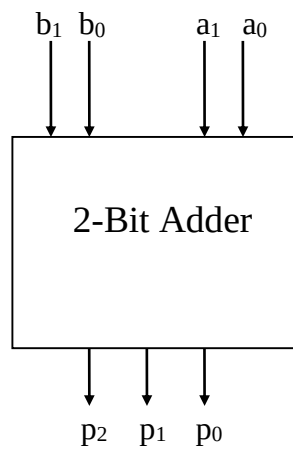


Figure Q4b

Design a logic circuit to perform this task without using Full adders or half adders

(19 marks)

4.

- a. Simplify the following expressions using De' Morgan's theorem and draw the resulting circuits in Sum of Products (SOP) form.

i. $L = \overline{\overline{A} \cdot B \cdot \overline{C}}$

ii. $M = \overline{A + B \cdot \overline{C}}$

iii. $N = A \cdot B \cdot \overline{(C \cdot D)}$

(6 marks)

- b. Design a counter, using D-type flip flops that repeatedly counts through the arbitrary sequence ...,0,1,5,7,9,11,13,0,1,5,7,9,11,13,....

(19 marks)