



School of Applied Computing ASSIGNMENT SPECIFICATION

Student name:	Joseph Potter	Student P number:	
Programme:	HND Electrical/Electronic Engineering		
Lecturer:	Jason Pointer	Internal Verifier:	Steve Roberts
Assignment Title:	Digital Circuits		
Hand Out Date:	23/03/18	Submission deadline:	11/05/18

Referencing:	In the main body of your submission you must give credit to authors on whose research your work is based. Append to your submission a reference list that indicates the books, articles, etc. that you have read or quoted in order to complete this assignment (e.g. for books: surname of author and initials, year of publication, <u>title of book</u> , edition, publisher: place of publication).		
Disclosure:	I declare that this assignment is all my own work and that I have acknowledged all materials used from the published or unpublished works of other people. All references have been duly cited.		
Student's Signature:	Hardcopy assignments will not be accepted without a signature here	Date:	

Late submission will result in a late penalty mark, as follows:

Up to one week late, maximum mark of 40% for first attempts and 0% for resubmissions.
(Academic Quality Handbook 2015/16 7.5 (5))

Learning Outcomes tested (from module syllabus)

1. Demonstrate an understanding of semi-conductor components and characteristics and their application in analogue and digital electronic circuits.

2. To design, simulate, build, test and evaluate analogue and digital electronic circuits using information gained from datasheets.

MARKING CRITERIA AND STUDENT FEEDBACK

This section details the assessment criteria. The *extent* to which these are demonstrated by you determines your mark. The marks available for each criterion are shown. Lecturers will use the space provided to comment on the achievement of the task(s), including those areas in which you have performed well and areas that would benefit from development/improvement.

Common Assessment Criteria Applied	Marks available	Marks awarded
1. Research-informed Literature Extent of research and/or own reading, selection of credible sources, application of appropriate referencing conventions.	10	4.5
References to a limited range of mostly relevant sources. Some omissions and minor errors.		
2. Knowledge and Understanding of Subject Extent of knowledge and understanding of contexts and underlying principles associated with the discipline	30	19
Knowledge is extensive. Exhibits very good understanding of digital circuits. Did not simplify the Boolean equations.		
3. Analysis Analysis, evaluation and synthesis, logic, argument and judgement, analytical reflection, organisation of texts and evidence	20	11
Evidence of some logical, analytical thinking. Has analyse new data and situations without guidance.		
4. Practical Application and Deployment Deployment of methods, materials, tools and techniques, application of concepts, formulation of innovative and creative solutions to solve problems	30	23
Excellent practical work, very little guidance was needed. All relative results were obtain and showed a clear understanding of the design work.		
5. Skills for Professional Practice Attributes in professional practice, individual and collaborative working, deployment of appropriate media, presentation and organisation	10	4.5
Work lacks coherence in places and could be better structured.		

Assignment Mark (Assessment marks are subject to ratification at the Exam Board. These comments and marks are to give feedback on module work and are for guidance only until they are confirmed.)

Late Submission Penalties (tick if appropriate)

Up to one week late

First Attempt?

✓

62%

Student Name: Joseph Potter

Student Number: 121306

Lecturer: Jason Pointer

Assignment: Digital Circuits

Module Code: PDSE4004

Assignment 3 of 3

Contents Page

Introduction _____	Page 3
Part 1 _____	Page 4 – Page 11
Part 2 _____	Page 12 – Page 13
Part 3 _____	Page 14 – Page 17
Part 4 _____	Page 18 – Page 19
Conclusion _____	Page 19
Bibliography _____	Page 20

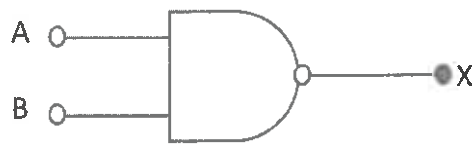
Introduction

This assignment is to focus on using NAND logic gates and logic circuits to construct each of the tasks from the given statements/diagrams and converting them to the simplest and most effective diagrams/truth table.

also include JKs

Task 1

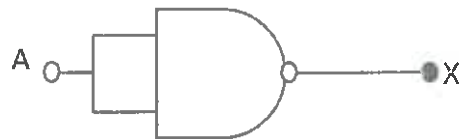
(a)



A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

$X = \overline{A \cdot B}$ NAND Gate

(b)

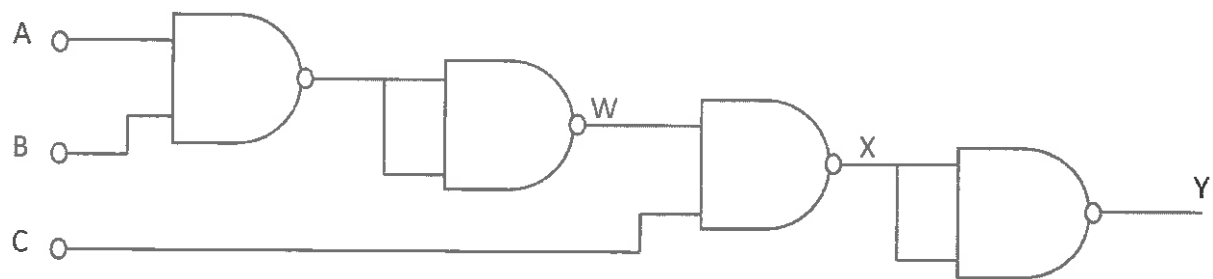


A	X
0	1
1	0

$X = \overline{A}$ NOT Gate

Need to state what you were doing

(c)



A	B	C	W	X	Y
0	0	0	0	1	0
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	0	1	0
1	0	0	0	1	0
1	0	1	0	1	0
1	1	0	1	1	0
1	1	1	1	0	1

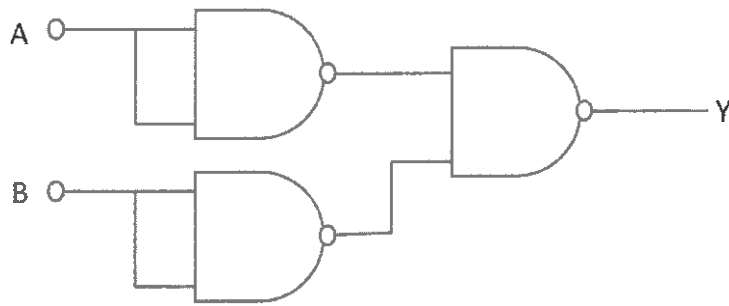
State the logic function for W, X and Y and simplify.

$W = A.B$ (2-input AND Logic Gate)

$X = \overline{A.B.C}$ (3-input NAND Logic Gate)

$Y = A.B.C$ (3-input AND Logic Gate)

(d)



A	B	X
0	0	0
0	1	1
1	0	1
1	1	1

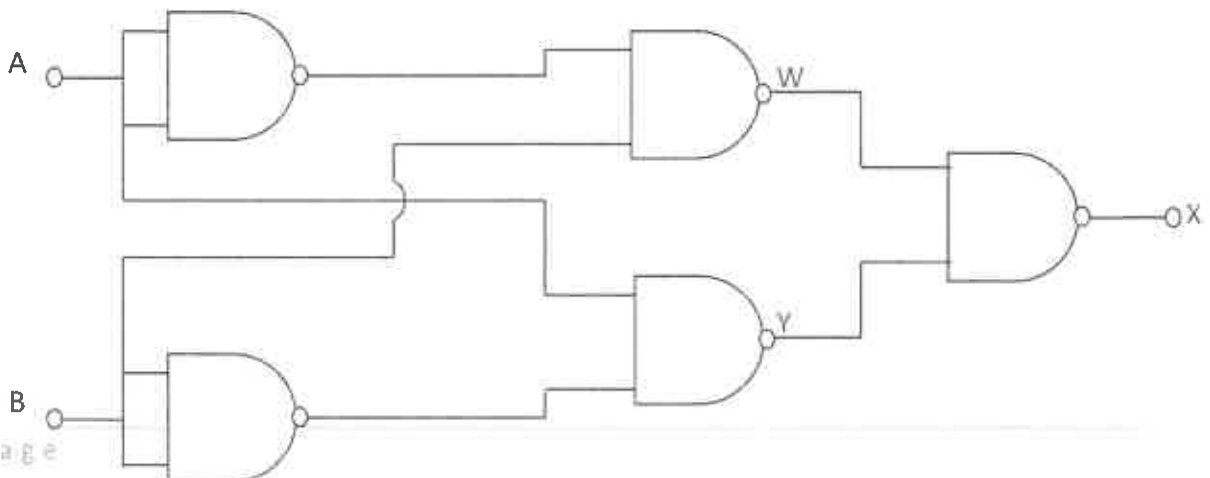
$X = A + B$ OR Gate

Circuit (b) is a NOT Gate, which inverts the output from Y in the diagram above, which will then turn the circuit into a NOR Gate.

A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

$X = \overline{A + B}$ NOR Gate

(e)



The circuit above was constructed.

A	B	W	Y	X
0	0	1	1	0
0	1	0	1	1
1	0	1	0	1
1	1	1	1	0

$$X = \bar{A}.B + A.\bar{B} = \text{XOR}$$

The theoretical value was the same as the measured values when the circuit was tested.

Part 1

Question 1

ECL or Emitter-Coupled Logic, is a logic family that uses high speed logic. There is a very low number of logic circuits that use ECL as these types of logic circuits as ECL continually draws current and power from the power supply more than other types of logic circuits.

CMOS or Complimentary MOS, draw a lot less power than ECLs and in doing so, see far more use. It is not uncommon to see these types of logic circuits in devices that can store information, sometimes the BIOS of a computer system can be housed inside of a CMOS logic circuit.

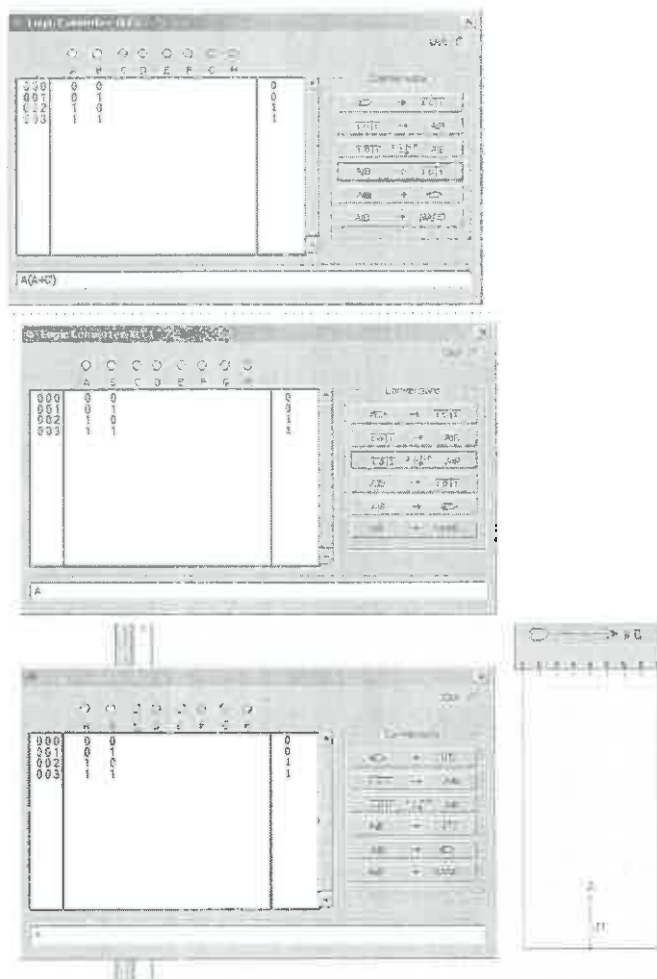
TTL or Transistor-Transistor Logic, is made of bipolar junction transistors, and are usually found in industrial controls and test equipment as they work better under stress than compared to that of the ECL or CMOS logic circuits, this is because they are built to withstand temperatures that would possibly break other types of logic circuits and this means that they last far longer.

Could have been more detailed re fan out etc

Question 2

Demorgans

i) $F = A(A + \overline{B})$



ii) $F = (A + B)(C + A)$

Logic Converter X01

	A	B	C	D	E	F	G	H
000	0	0	0	0	0	0	0	0
001	0	0	0	1	0	0	0	0
002	0	0	1	0	0	0	0	0
003	0	0	1	1	0	0	0	0
004	0	1	0	0	0	0	0	0
005	0	1	0	1	0	0	0	0
006	0	1	1	0	0	0	0	0
007	0	1	1	1	0	0	0	0

(A+B)(C+A)

Logic Converter X02

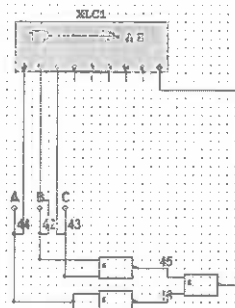
	A	B	C	D	E	F	G	H
000	0	0	0	0	0	0	0	0
001	0	0	0	1	0	0	0	0
002	0	0	1	0	0	0	0	0
003	0	0	1	1	0	0	0	0
004	0	1	0	0	0	0	0	0
005	0	1	0	1	0	0	0	0
006	0	1	1	0	0	0	0	0
007	0	1	1	1	0	0	0	0

BC+A

Logic Converter X03

	A	B	C	D	E	F	G	H
000	0	0	0	0	0	0	0	0
001	0	0	0	1	0	0	0	0
002	0	0	1	0	0	0	0	0
003	0	0	1	1	0	0	0	0
004	0	1	0	0	0	0	0	0
005	0	1	0	1	0	0	0	0
006	0	1	1	0	0	0	0	0
007	0	1	1	1	0	0	0	0

BC+A



iv) $F = (\bar{A} + \bar{B} + \bar{C})(A + \bar{B} + \bar{C})(A + C)(B + \bar{C})$

Logic Converter 31.2

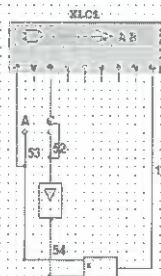
	A	B	C	D	E	F	G	H
000	0	0	0					0
001	0	0	1					0
002	0	1	0					0
003	0	1	1					0
004	1	0	0					0
005	1	0	1					0
006	1	1	0					0
007	1	1	1					0

$(A + B + C)(A + B + C)(A + C)(B + C)$

Logic Converter 31.3

	A	B	C	D	E	F	G	H
000	0	0	0					0
001	0	0	1					0
002	0	1	0					0
003	0	1	1					0
004	1	0	0					0
005	1	0	1					0
006	1	1	0					0
007	1	1	1					0

AC



Logic Converter 31.4

	A	B	C	D	E	F	G	H
000	0	0	0					0
001	0	0	1					0
002	0	1	0					0
003	0	1	1					0
004	1	0	0					0
005	1	0	1					0
006	1	1	0					0
007	1	1	1					0

AC

You have not simplified using Boolean

Part 2

- (a) Binary Coded Decimal (BCD) is a 4-bit binary code with the range of numbers 1010 to 1111 not used. Design a circuit that will detect these invalid codes. Construct the circuit and verify that it performs the required task.

A	B	C	D	X
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

		CD			
		0	1	11	10
AB	0	0	0	0	0
	1	0	0	0	0
	11	1	1	1	1
	10	0	0	1	1

$$X = A \cdot \bar{B} \cdot C \cdot \bar{D} + A \cdot \bar{B} \cdot C \cdot D + A \cdot B \cdot \bar{C} \cdot \bar{D} + A \cdot B \cdot \bar{C} \cdot D + A \cdot B \cdot C \cdot \bar{D} + A \cdot B \cdot C \cdot D$$

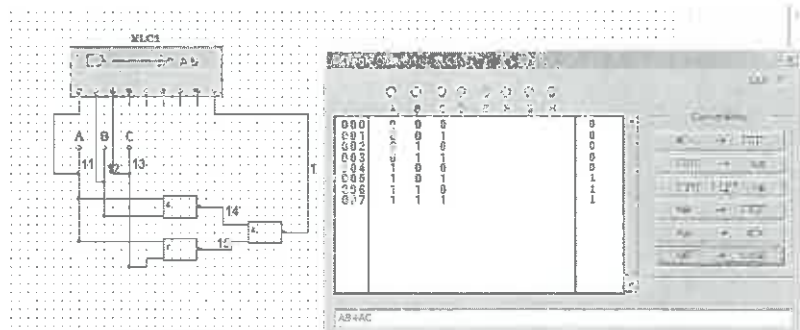
DeMorgans

$$X = A \cdot C + A \cdot C$$

$$\bar{X} = \overline{A \cdot B + A \cdot C}$$

$$\bar{X} = \overline{(A \cdot B) \cdot (A \cdot C)}$$

$$X = \overline{(A \cdot B) \cdot (A \cdot C)}$$



For Part 2(a), the above circuit was constructed and the Karnaugh map was designed to simplify the equation. The equation was then input into Multisim to provide a simplified circuit. The simulated circuit agrees with design requirements.

- (b) Design a 2-bit comparator whereby the output is HIGH when the one of the two-bit number is equal to or greater than a second two-bit number.

Bit 1		Bit 2		X
A	B	C	D	
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

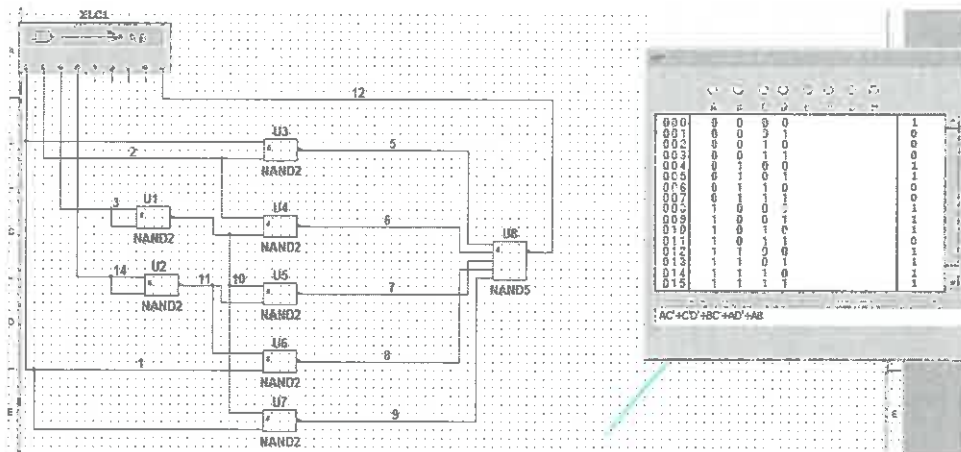
$$X = \bar{C}.\bar{D} + A.\bar{D} + A.\bar{C} + A.B + B.\bar{C}$$

		CD			
		00	01	11	10
AB	00	1	0	0	0
	01	1	1	0	0
	11	1	1	1	1
	10	1	1	0	1

DeMorgans

$$\bar{X} = \overline{\bar{C}.\bar{D} + A.\bar{D} + A.\bar{C} + A.B + B.\bar{C}}$$

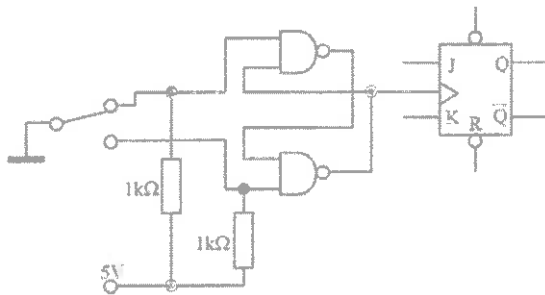
$$\bar{X} = (\bar{C}.\bar{D}).(\overline{A.\bar{D}}).(\overline{A.\bar{C}}).(\overline{A.B}).(\overline{B.\bar{C}})$$



For Task 2(b), the circuit was constructed with aid of a table to show how the results would look, and then using the equations gathered from the table to create a Karnaugh map, then using the simplified equation to construct the circuit. The circuit was simulated and the comparator worked correctly.

Part 3

(a) The circuit below was constructed.



(b) The results for the following table were recorded and the logic 1 in the Q and $\bar{Q}$, means that the corresponding part of the J-K flip-flop was on.

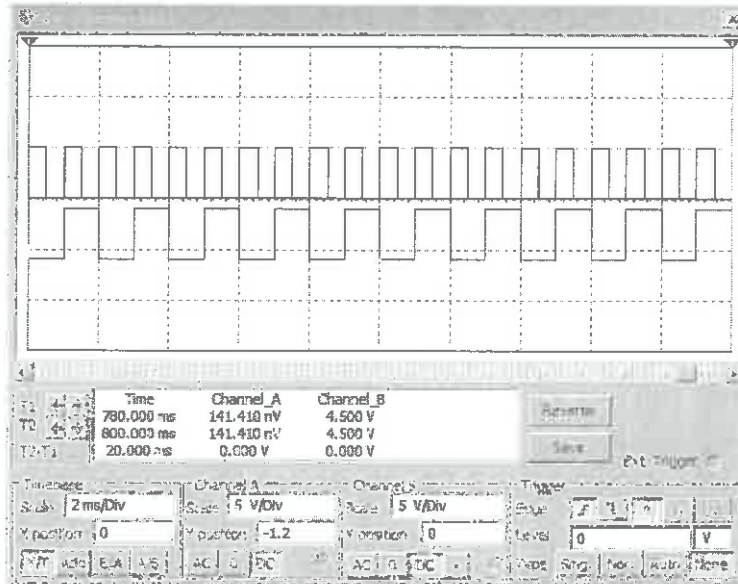
Inputs					Outputs	
Preset (S)	Clear (R)	Clock	J	K	Q	$\bar{Q}$
0	1	x	x	x	1	0
1	0	x	x	x	0	1
0	0	x	x	x	1	0
1	1		L	L	1	0
1	1		H	L	1	0
1	1		L	H	0	1
1	1		H	H	1	0

(c)

- The significant details about the output state "Preset = Clear = Logic '0'" is that, when logic equals 0, it signifies that Q is on and not Q is off, this is usually done as a test to see if the JK is faulty.
- The JK flip-flops used in this assignment are negative edged, meaning that each clock triggers on the logic 0 of the clock.
- On the negative edge of the clock.
- The SN7476 has a trigger action on a negative edge.
- To stop the clock pulse from bouncing a debounce switch would be in place to stop the clock pulse from closing. As stated in *The Art of Electronics, Horowitz & Hill, Second edition, pg 506* : "When the switch is closed, the two contacts actually separate and reconnect, typically 10 to 100 times over a period of about 1ms." In the example written from "*The art of Electronics*", a debouncing switch would prolong the length of time for the switch to close/open.

(d)

- i) The clock circuit was replaced with a TTL signal generator.
- ii) The generator was set to 1kHz and the preset was set so that there was a logic = 1.

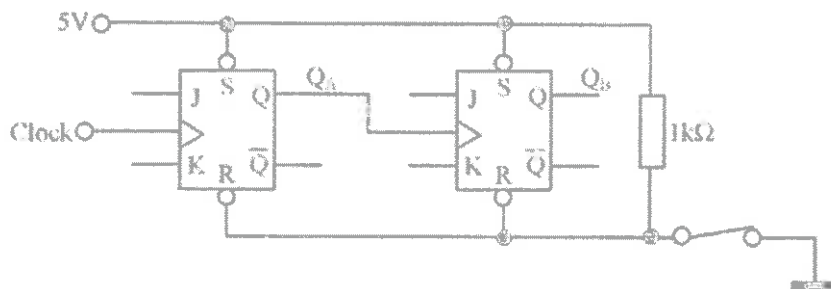


iii)

The above results were recorded and displayed on an oscilloscope. The waveform above shows that the Q output turns on and off in correspondence to the clock pulse.

(e) Asynchronous Counters

- i) The circuit below was constructed to and they were both set to logic 1.

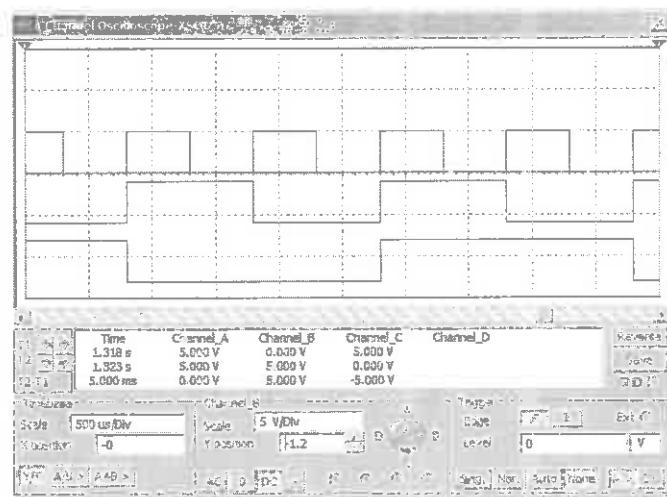


- ii) The Q outputs were connected to LEDs to show that the JK flip flops were both at logic 1.

iii) The following table of results were tested and recorded after clearing the counter.

Table 3(a)			Table 3(b)	
Pulse	QA	QB	QA	QB
Clear	0	0	0	0
1	1	1	1	0
2	0	1	0	1
3	1	0	1	1
4	0	0	0	0
5	1	1	1	0

iv)



The clock pulse diagram above shows that QB turns on and off when the clock pulse and QA turn on. This shows that the circuit is counting down from 11.

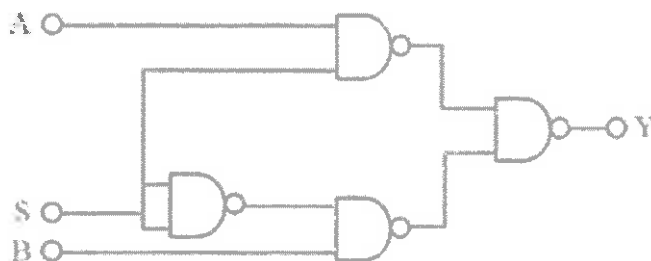
v)



From the above waveform and the waveform in part 3 (e) (iv), it can be seen that QB switches off and on in accordance with the clock pulse. The biggest difference within the two waveforms is the starting position. This waveform is counting up, whereas the one in part 3 (e) (iv) is counting down.

f)

i)



The above circuit was constructed.

ii)

S=1

A	B	Y
0	0	0
0	1	0
1	0	1
1	1	1

S=0

A	B	Y
0	0	0
0	1	1
1	0	0
1	1	1

The circuit was built and counts up and down when S is equal to 1 or 0.

Part 4

Design and simulate a 3-stage synchronous binary counter that will produce the odd numbers (including zero) in the range 0 to 7.

Present Q	Next Q	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Present			Next			Input					
Qa	Qb	Qc	Qa	Qb	Qc	Ja	Ka	Jb	Kb	Jc	Kc
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	1	0	X	1	X	X	0
0	1	1	1	0	1	1	X	X	1	X	0
1	0	1	1	1	1	X	0	1	X	X	0
1	1	1	0	0	0	X	1	X	1	X	1

Ja		Qb/Qc			
		00	01	11	10
Qa	0	0	0	1	X
	1	X	X	X	X

Ja=Qb

Ka		Qb/Qc			
		00	01	11	10
Qa	0	X	X	X	X
	1	X	0	1	X

Ka=Qb

Jb		Qb/Qc			
		00	01	11	10
Qa	0	0	1	X	X
	1	X	1	X	X

Jb=Qc

Kb		Qb/Qc			
		00	01	11	10
Qa	0	X	X	1	X
	1	X	X	1	X

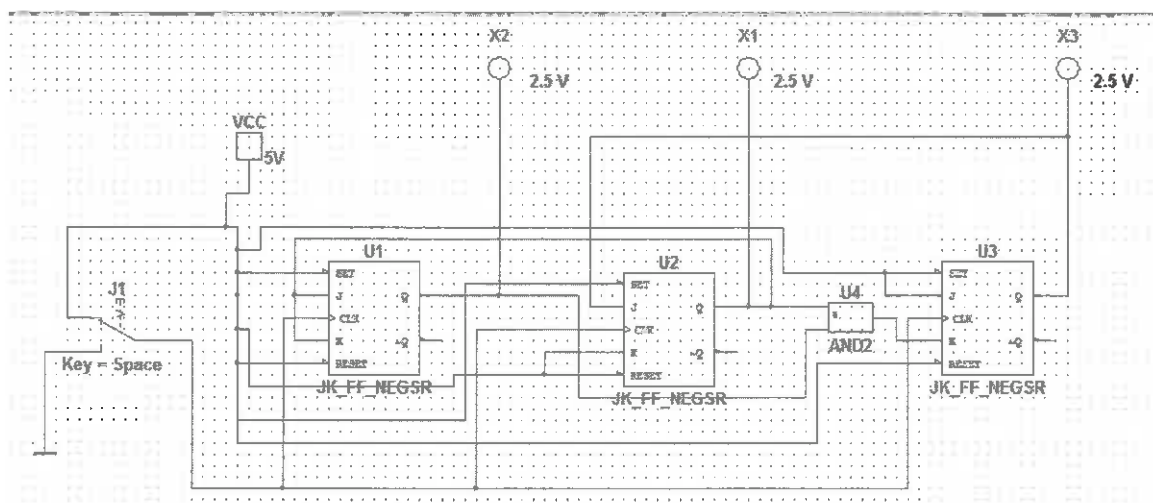
Kb=1

Jc		Qb/Qc			
		00	01	11	10
Qa	0	1	X	X	X
	1	X	X	X	X

Jc=1

Kc		Qb/Qc			
		00	01	11	10
Qa	0	X	0	0	X
	1	X	0	1	X

Kc=Qa.Qb



The circuit was constructed on Multisim and the circuit functions correctly according to the truth table.

Conclusion

In conclusion, the circuits in this assignment were designed and simulated from their most complicated structures, to the simplest structure of each section.

Very brief conclusion

Bibliography

Bird. J (2007) *Electrical and Electronic Principles and Technology* 3rd edition. Oxford. Newnes

Brock J. (2017) *Introduction to Logic Circuits & Logic Design with VHDL*.

Johnson. D.H (2016) *Fundamentals of Electrical Engineering I*. Houston. Rice University

National Extension College Trust Ltd. *Introducing Transistors*

P. Horowitz and H. Winfield (1990) *The Art of Electronics* 2nd Edition. Cambridge. Press Syndicate of the University of Cambridge

This was a reference

Uyemura J.(2001) *CMOS Logic Circuit Design*. Springer

You have cover all the practical elements and design work. In places your comments could have been more detailed