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by Matthew Davies

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Good list of tables

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Good organised table of contents

1. Executive Summary

This assignment explored topic areas covering the range of manufacturing processes and techniques of Integrated Circuits (IC's) and the fault modelling techniques employed during the design and testing procedure for confirmation of operation. Modern manufacturing techniques and wider engineering requirements were explored via systems such as machine vision and in-circuit testing. As well as this, the dangers of electrostatic discharge were explored and the methods used to prevent it from happening.

The IC required 6 inputs and 1 output to perform a specific function. This was designed using a series of Karnaugh maps and truth tables to determine the circuit construction and operation. Fault modelling techniques such as the 'stuck at' method were employed to detect faults on the prototype during testing. The prototype was designed on multisim, and then also on LabView. These programs allowed it to be simulated and tested virtually, before building the prototype on the NI Elvis board to test the circuit physically. The results from these tests were recorded, compared, and evaluated against the research carried out at the beginning of the assignment before determining whether the circuit was operating correctly or not. These tests were successful and allowed the PCB design to be exported to a company for production.

Summary could be more detailed for the same word count

2. Research

Integrated Circuit Fabrication Faults

Due to the nature of Integrated Circuit (IC) fabrication the IC's can fail. This can be down to impurities and contaminants in the silicon, crystal defects or design problems during the fabrication. (Holland, 2019) These defects can be presented as short or open circuits on the boards where unwanted etching on the conductive material may have occurred, dust particles may have appeared which would cause issues with photolithography and a possibility of chemical deposits remaining from the fabrication.

According to (Mack, 2020) photolithography is a manufacturing process that uses a light sensitive polymer (photoresist) to form a 3D relief image on the substrate. The lithography manufacturing process is shown below in Figure 1. This is a wafer-thin material which has complex circuits printed onto it with the use of conductors and insulators for the connection of electronic components.

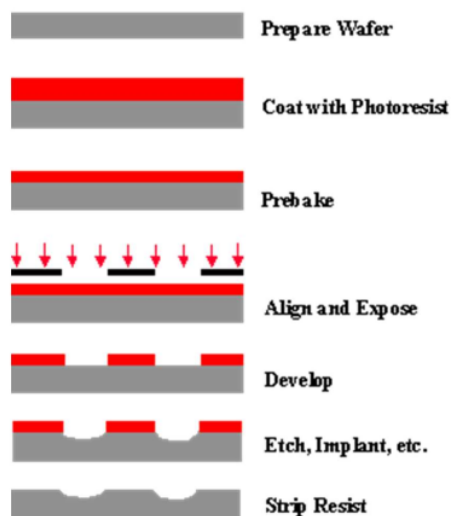


Figure 1 - Lithographic processing steps

Another common fault which can be found with IC's is electrical overstress. This occurs when the device is exposed to voltage levels of magnitude of which it cannot stand. This could be caused due to power surges or because of misuse and neglect by using the application incorrectly according to the specification. (Trompert, 2020)

Good explanation with supporting images

As part of this assignment, single stuck at faults are being investigated and are a very common fault in IC's. Single stuck at faults can be defined as:

- One line or wire being faulty.
- Faulty line permanently set to 0 or 1.
- Can be at the input or output of gate.

To test faults such as these, test vectors are used. These are patterns which can be applied to a circuit to detect a certain fault which has been placed on a circuit. To test the pattern, the output of the circuit must be different to that of the good circuit to successfully test it. (Meixner, 2023)

The 4 types of stuck at faults are:

- Stuck at 1 (SA1): where the input or output is stuck at logic 1.
- Stuck at 0 (SA0): where the input or output is stuck at logic 0.
- Feedback bridging fault: input/output of gate is shorted.
- Bridging fault: two outputs of gate(s) shorted together.

A schematic showing these faults can be seen below in Figure 2. (Starzyk & Liu, 2002)

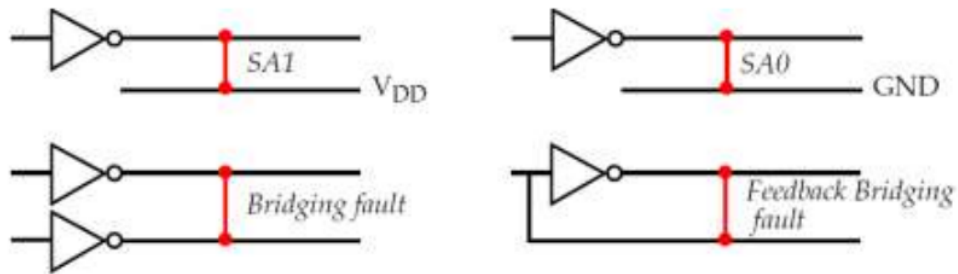


Figure 2 - Stuck at faults.

Good research on different types of SSF

Electrostatic Discharge

Electrostatic discharge (ESD) occurs when a potential difference is created when two objects come into contact with each other. It occurs when two dissimilar materials rub together, and one material becomes positively charged and the other becomes negatively charged. When the positively charged material touches a specific type of material, the charge is transferred and an ESD event occurs. (TechTarget, 2020)

ESD can cause damage to integrated circuits (IC) if they are not protected sufficiently against the discharges. If the IC cannot withstand the high voltages produced from the ESD, then the discharge will cause severe damage to the components and will likely discharge through the gate oxide, as this is the most susceptible to these kinds of problems. The components will be crossing their operating thresholds regularly and will degrade and break down eventually. An example of this is shown in Figure 3. Due to the smaller nature of ICs in the modern world, there is now a lot smaller surface area for the ESD to discharge through, in turn causing the components to take a higher amount of discharge. (Toms, et al., 2015)

To prevent the damage that ESD can cause, there are several methods available to use that will minimise the likelihood and severity. For example, if a worker was working on an electronic circuit with their bare hands, they should wear a grounding wrist strap to provide the lowest impedance path for the current to flow. Grounding and antistatic mats are also widely used to protect the equipment and users. (Turley, et al., 2013) When components which are electrostatic sensitive are in transit for example, they will often be placed in antistatic bags for packaging. These are typically made from polyethylene terephthalate as they won't conduct the discharge. Also, antistatic sprays are used to prevent the accumulation of charges on the equipment, especially when they are moving at high speeds which can be difficult to block the ESD effects. (Cadence Systems, 2021)



Good research on ESD and preventive measures. Application examples could have been included to support the preventive measures research

Figure 3 - ESD damage to a PCB (Peterson, 2017)

Manufacturing methods and testing procedures for wider engineering practices

To manufacture a sustainable product whilst meeting wider engineering requirements, a typically new method of monitoring machinery is using 'machine vision systems'. These are assemblies of integrated circuits, software algorithms and computer hardware to produce a sustainable product by processing images captured from the operational process. From the data obtained from the machine vision system, the system can become automated to control how the product is produced and inspected. For example, it can detect the condition of the products and then either rectify faults, dispose of the products, or allow them to carry on down the processing line if there are no faults. (IQS directory, 2020)

To test the integrated circuits which would typically be used in systems such as machine vision, a testing machine called a 'bed of nails test fixture' can be used. This is a traditional electronic test fixture which uses several pins (nails) which are inserted into holes in an epoxy phenolic glass cloth laminated sheet. (Bittele Electronics, 2020) Using tooling pins, they are aligned to make contact with the test points on the PCB and connect to the measuring unit with a pair of wires. Each nail on the bed makes contact with a single node on the CUT (Circuit Under Test) by pressing the CUT against the bed of nails, where the contact can be made quickly and reliably, with a vacuum pulling the CUT onto the bed of nails. (Professional Plastics, 2019) An image of a bed of nails tester can be seen in Figure 4 below.

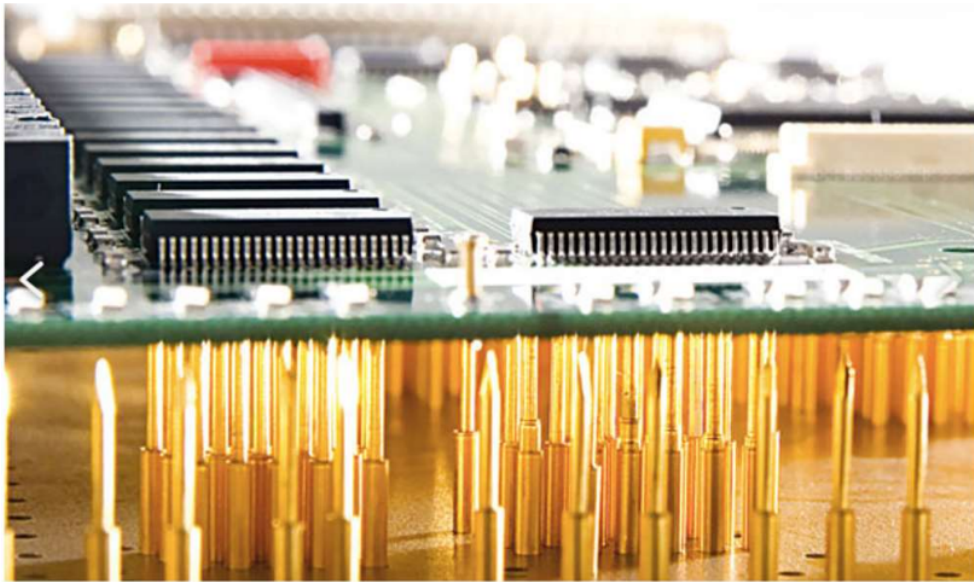


Figure 4 - Bed of Nails tester (Cockfield, 2019)

Good points identified with relevant source

There are wider areas to investigate here, such as frequency signature recognition which is becoming popular with contactless sensing topic areas.

3. Design of assignment requirements

The circuit below in Figure 5 was created on Multisim, which is an ECAD software. This circuit will be the circuit under test (CUT) for the test and analysis. To meet the specification, the combinational circuit has 4 gates, 6 inputs and 1 output to provide the specific function to the customers' requirement.

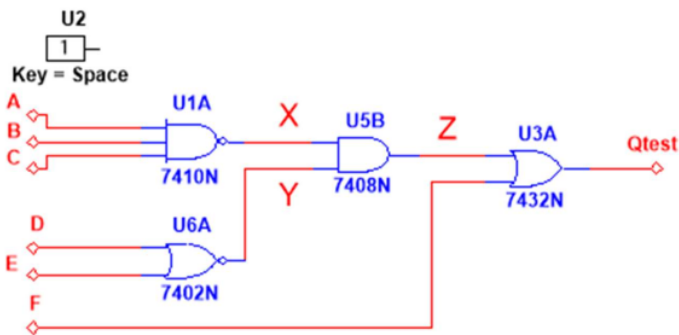


Figure 5 - Circuit Under Test

3.1 Stuck at Fault Modelling

This fault modelling technique was implemented to detect faults where the inputs were either stuck at logic 0 (SA0) or logic 1 (SA1). This test was carried out for each logic gate on the combinational circuit.

To calculate the number of tests required for each gate, the following formula was used:

$$\text{No. of tests} = m + 1$$

Where m = number of inputs to the gate.

Figure 6 shows the inputs and output from the 3 input NAND gate, as well as a table showing the 4 tests and their expected results.

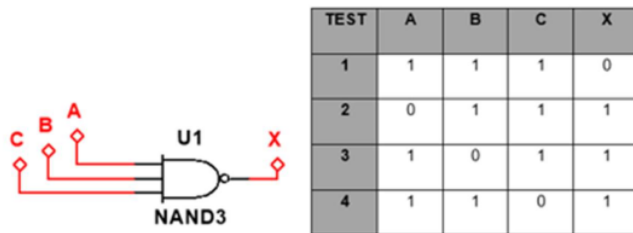


Figure 6 - Reduced test 3 input NAND gate

Figure 7 shows the 2 input NOR gate with a table for expected test results.

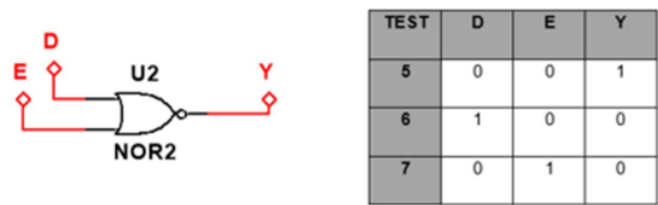


Figure 7 - Reduced test 2 input NOR gate

Figure 8 shows the 2 input AND gate and the testing table.

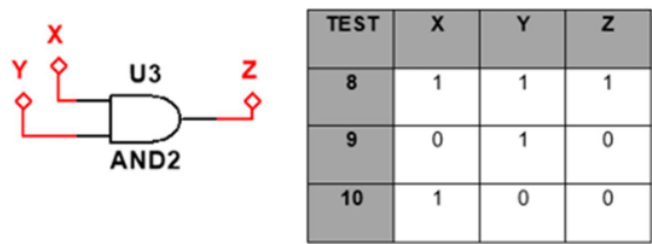


Figure 8 - Reduced test 2 input AND gate

Figure 9 shows the 2 input OR gate and the testing table.



Good redundancy methods used for each logic gate

Figure 9 - Reduce test 2 input OR gate.

3.2 Test vector truth tables and possible faults

Table 1 below is the derived table for the potential stuck at fault tests and the fault scenario required for testing each stage. This table is an amalgamation of the testing tables in section 3.1 previously.

Test	A	B	C	D	E	F	Qgood	HEX	X	Y	Z	Fault
1	1	1	1	0	0	0	0	70	0	1	0	A+B+C SA0
2	0	1	1	0	0	0	1	31	1	1	1	A SA1
3	1	0	1	0	0	0	1	51	1	1	1	B SA1
4	1	1	0	0	0	0	1	61	1	1	1	C SA1
5	0*	0*	0*	0	0	0	1	01	1	1	1	D+E SA1
6	0*	0*	0*	1	0	0	0	08	1	0	0	D SA0
7	0*	0*	0*	0	1	0	0	04	1	0	0	E SA0
8	0*	0*	0*	0	0	0	1	01	1	1	1	X+Y SA0
9	1	1	1	0	0	0	0	70	0	1	0	X SA1
10	0*	0*	0*	1**	1**	0	0	0C	1	0	0	Y SA1
11	1	1	1	1**	1**	0	0	7C	0*	0*	0	F+Z SA0
12	1	1	1	1**	1**	1	1	7F	0*	0*	0	F SA0
13	0*	0*	0*	0	0	0	1	01	1	1	1	Z SA0

Table has been created from the theory of SSF modelling

Table 1 - Derived Table

In Table 1, certain inputs on the table have either a * or ** next to them. These are called wildcards. * Means that at least 1 of the inputs must be logic 0, and ** means at least 1 of the inputs must be logic 1. [Significant key rule is identified here.](#)

The rows of tests which are shaded in either red or yellow mean that the tests have been duplicated, therefore meaning they can be removed from the table and reduce the number of tests required. This can be seen on the following page as Table 2.

Test	A	B	C	D	E	F	Qgood	HEX	X	Y	Z	Fault
1	1	1	1	0	0	0	0	70	0	1	0	A+B+C SA0, X SA1
2	0	1	1	0	0	0	1	31	1	1	1	A SA1
3	1	0	1	0	0	0	1	51	1	1	1	B SA1
4	1	1	0	0	0	0	1	61	1	1	1	C SA1
5	0*	0*	0*	0	0	0	1	01	1	1	1	D+E SA1, X+Y SA0, Z SA0
6	0*	0*	0*	1	0	0	0	08	1	0	0	D SA0
7	0*	0*	0*	0	1	0	0	04	1	0	0	E SA0
10	0*	0*	0*	1**	1**	0	0	0C	1	0	0	Y SA1
11	1	1	1	1**	1**	0	0	7C	0*	0*	0	F+Z SA1
12	1	1	1	1**	1**	1	1	7F	0*	0*	0	F SA0

Table 2 - Reduced Table

Due to test 5 having wildcards, the inputs can be changed to match test 4, meaning test 5 can be eradicated, as well as test 10's wildcards being altered to match test 6, so test 10 can be removed too.

The final reduction table can be seen below (Table 3) where 8 test vectors are remaining.

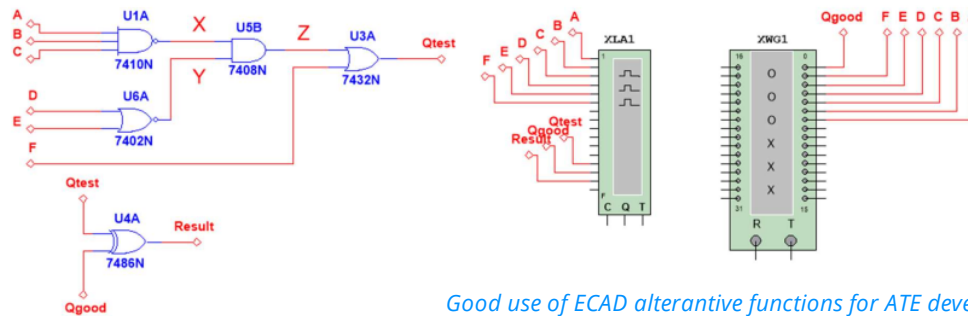
Test	A	B	C	D	E	F	Qgood	HEX	X	Y	Z	Fault
1	1	1	1	0	0	0	0	70	0	1	0	A+B+C SA0, X SA1
2	0	1	1	0	0	0	1	31	1	1	1	A SA1
3	1	0	1	0	0	0	1	51	1	1	1	B SA1
4	1	1	0	0	0	0	1	61	1	1	1	C SA1, D+E SA1, X+Y SA0, Z SA0
6	0*	0*	0*	1	0	0	0	08	1	0	0	D SA0, Y SA1
7	0*	0*	0*	0	1	0	0	04	1	0	0	E SA0
11	1	1	1	1**	1**	0	0	7C	0*	0*	0	F+Z SA1
12	1	1	1	1**	1**	1	1	7F	0*	0*	0	F SA0

Table 3 - Final reduction table

Good reduction methods used by applying the wildcard rule to further reduce the number of test vectors.

3.3 Design test using word generator.

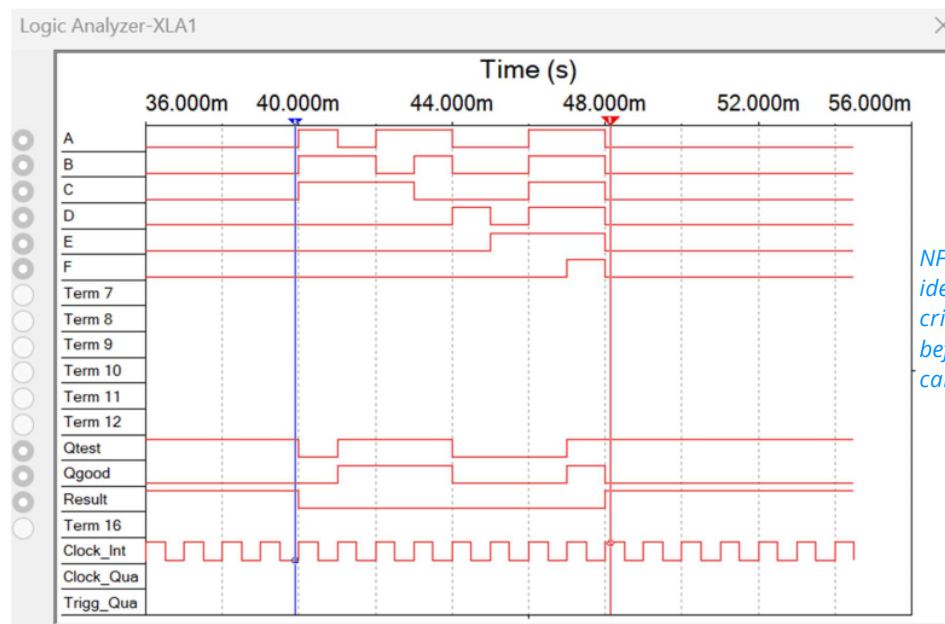
Figure 10 below shows the Automatic Test Equipment (ATE) for the circuit under test (CUT). This uses a word generator on multisim to generate a test sequence for the inputs to the circuit.



Good use of ECAD alternative functions for ATE development. This demonstrates a good understanding of requirements

Figure 10 - CUT ATE Test Circuit

The results from the simulation were taken from the logic analyser, which is labelled as 'XLA1' in Figure 10. The results below in Figure 11 show there was no fault found in this test, as the line labelled as 'Result' in the graph below doesn't have a positive pulse between the 2 cursors. This is correct operation of the test as no 'stuck at' faults were implemented.



NFF condition is identified. This is a critical state to achieve before testing can be carried out.

Figure 11 - No Fault Found Multisim

4. Analysis of NI Multisim results

The circuit in Figure 10 was used to test the fault conditions which were derived in Table 3 and to prove that the faults would provide the expected result by using the logic analyser. 3 faults from Table 3 were put on the circuit, as explained in this following section.

4.1 Fault - A stuck at 0.

The first test circuit is shown below in Figure 12 where input A was tested to be stuck at logic 0.

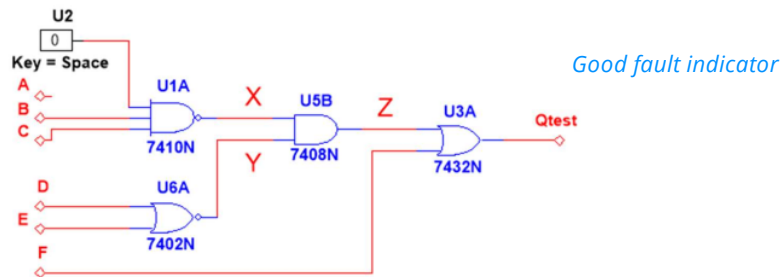


Figure 12 - A stuck at 0.

Figure 13 below shows the fault as the 'result' line should've gone to logic 0 where the blue cursor is, as opposed to staying at logic 1 as its default.

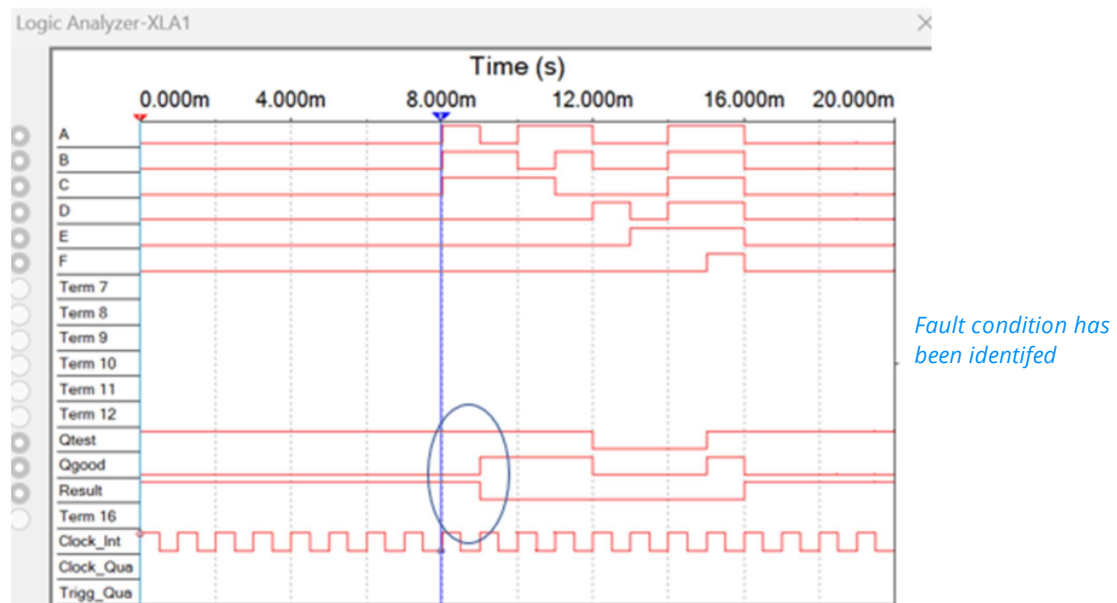


Figure 13 - A stuck at 0 graph.

4.2 Fault – C stuck at 1.

The testing circuit for C stuck at 1 can be seen below in Figure 14 where C is friggid to be stuck at 1.

*Do not use this word.
Alternative words are:
altered, changed or
reconfigured.*

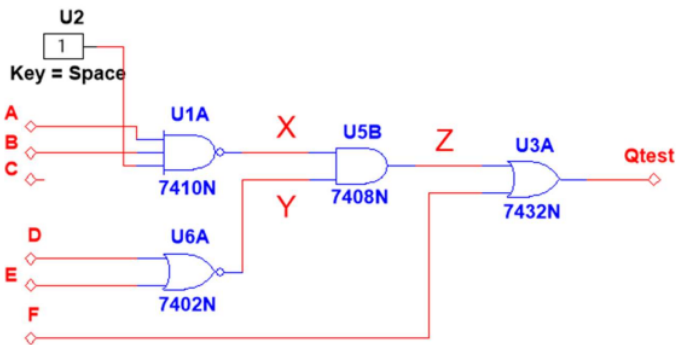


Figure 14 - C stuck at 1.

The graph to show the fault condition is below in Figure 15. The fault is shown in the circled area, where the result line pulses just after C was meant to go back to logic 0 instead of being stuck at logic 1.

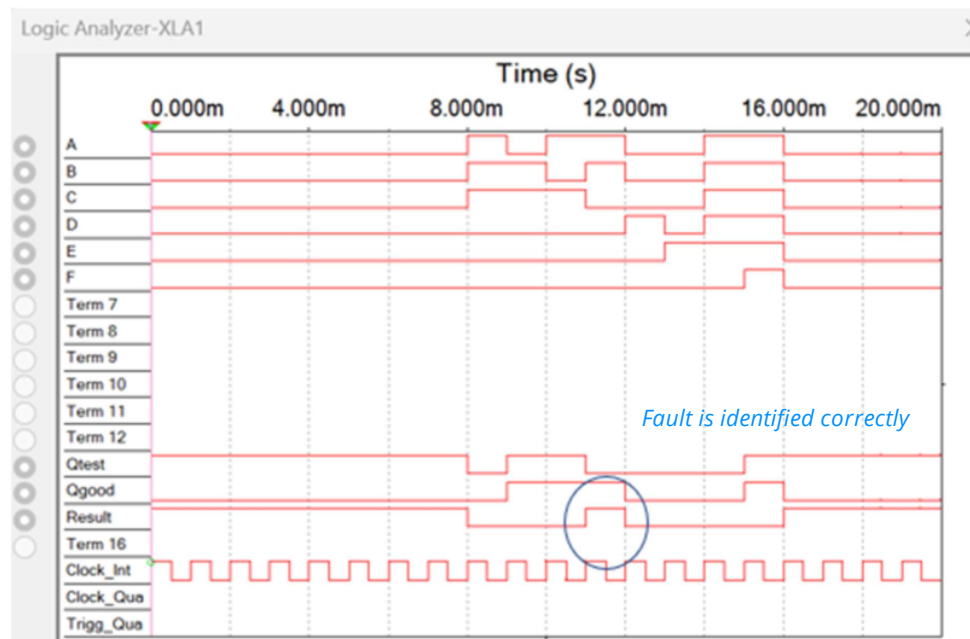


Figure 15 - C stuck at 1 graph.

4.3 Fault – D stuck at 0.

The testing circuit for D stuck at 0 can be seen below.

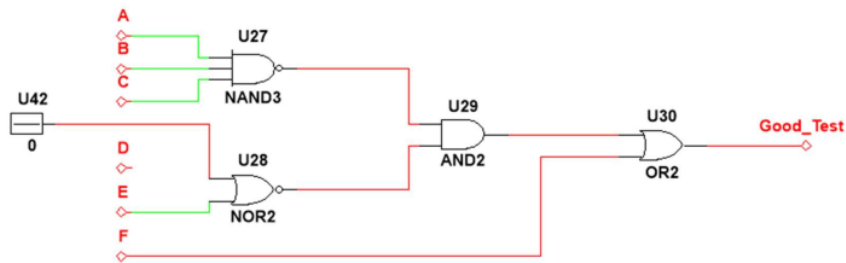


Figure 16 - D stuck at 0.

The graph below shows the fault occurred and the testing circuit responded correctly. This is shown in the circled area on the graph in Figure 17, where the result line pulses when the D input is meant to go to 1 but is stuck at 0.

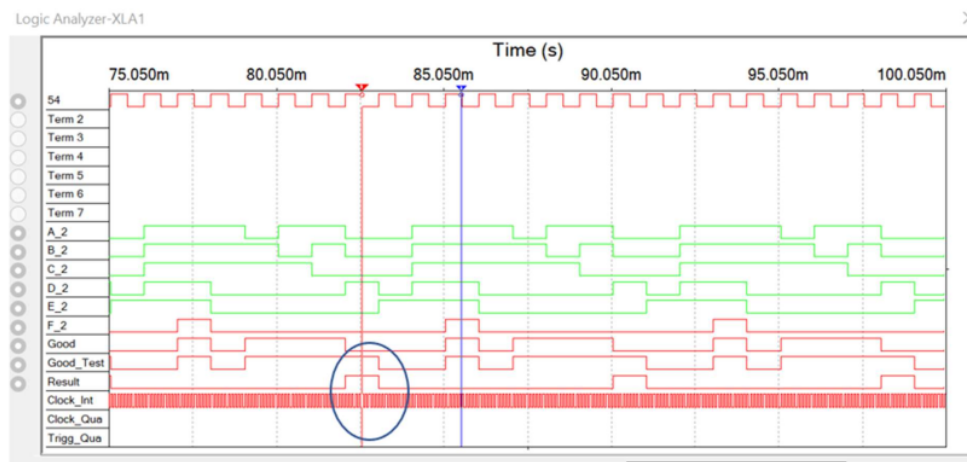


Figure 17 - D stuck at 0 graph.

Fault condition evidence and associated test results have been explained.

5. Practical build and test using LabVIEW.

5.1. 6-Bit Register Design and Test

This section is not using LabVIEW

For testing the CUT, a 6-bit pattern generator was designed and used as part of the ATE design. To design this finite state machine, a truth table with the present and next states had to be designed as seen in Table 4. This allowed the test vectors for inputs A to F to be produced.

Present State						Next State					
A	B	C	D	E	F	A+	B+	C+	D+	E+	F+
1	1	1	0	0	0	0	1	1	0	0	0
0	1	1	0	0	0	1	0	1	0	0	0
1	0	1	0	0	0	1	1	0	0	0	0
1	1	0	0	0	0	0	0	0	1	0	0
0	0	0	1	0	0	0	0	0	0	1	0
0	0	0	0	1	0	1	1	1	1	1	0
1	1	1	1	1	0	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	0	0	0

Table 4 - 6 Bit Generator Next State Table

Next state table is correct

To generate the logic states required for the feedback combinational logic for the input sequence, Karnaugh maps were used. All these Karnaugh maps can be seen in Appendix 9.1. Karnaugh maps.

The Boolean expressions derived from these Karnaugh maps can be seen below.

$$\text{Output QA} = A.B.C.D.E + A.NB.C.ND.NE.NF + NA.B.C.ND.NE.NF + NA.NB.NC.ND.E.NF$$

$$\text{Output QB} = A.C.ND.NE.NF + A.B.C.D.E + NA.NB.NC.ND.E.NF$$

$$\text{Output QC} = NA.NB.NC.ND.E.NF + NA.B.C.ND.NE.NF + A.B.C.ND.NE.NF + A.B.C.D.E$$

$$\text{Output } QD = NA.NB.NC.ND.E.NF + A.B.NC.ND.NE.NF + A.B.C.D.E.NF$$

$$\text{Output } QE = NA.NB.NC.ND.E.NF + NA.NB.NC.D.NE.NF + A.B.C.D.E.NF$$

$$\text{Output } QF = A.B.C.D.E.NF$$

Using the results from the next state logic design procedure, the 6-bit register was produced using multisim and can be seen below in Figure 18. The CUT is part of the circuit shown below, and the output from the CUT is compared to the output of a known source. To differentiate between the 2 circuits, the output from the CUT and the known source go into an XOR gate.

Good identification of X-OR function

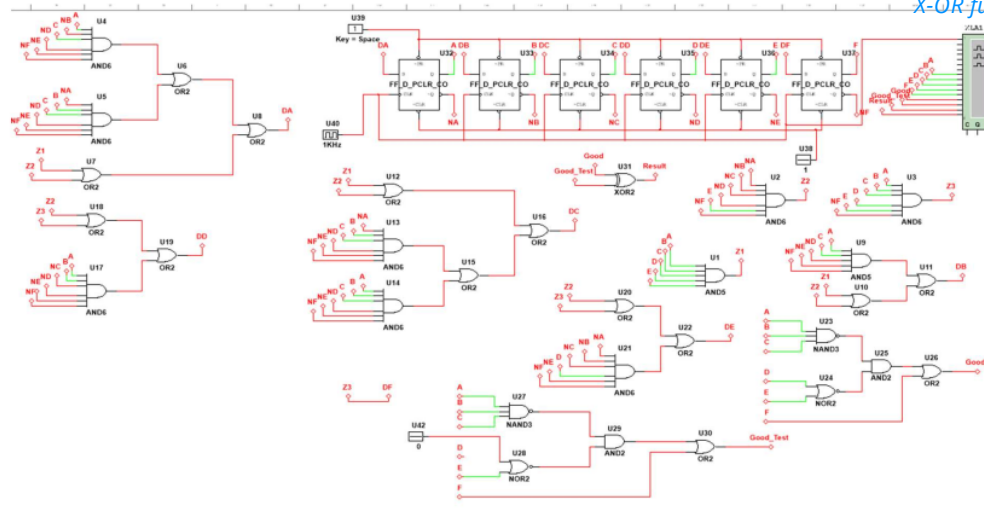
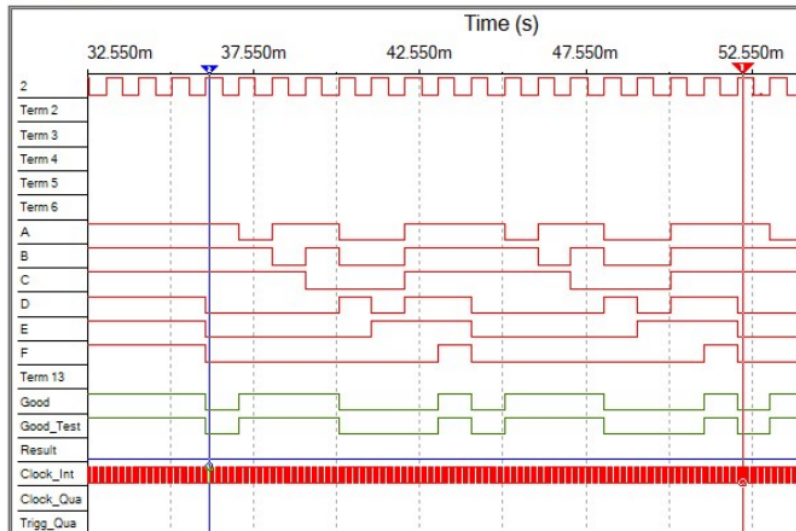


Figure 18 - 6 Bit Register

The circuit was tested with no fault condition initially. The result from this is shown below in Figure 19. The circuit behaved as expected, as the 'result' line didn't produce a pulse. This line is the output from the XOR gate.

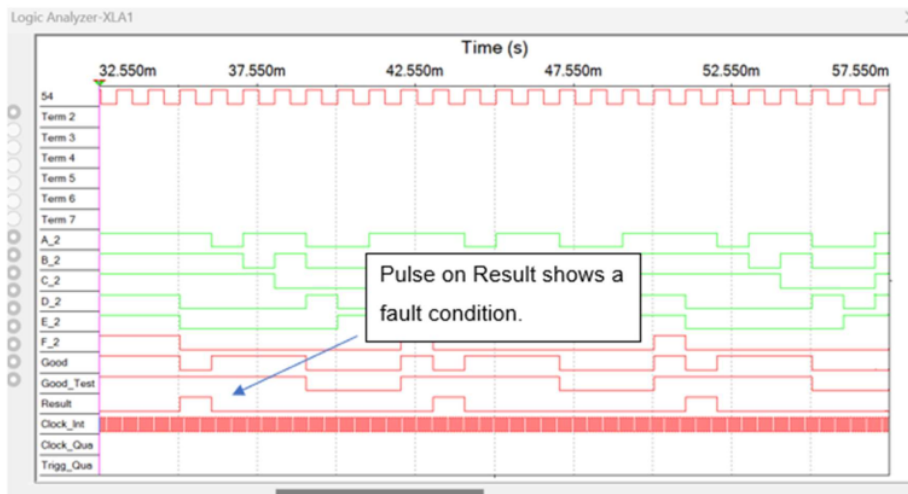
ic Analyzer-XLA1



*NFF condition is achieved.
Critical before carrying out
further tests*

Figure 19 - ATE no fault condition.

The CUT ATE was then tested with the input A stuck at 0. The graph below proves that it is functioning correctly as the 'result' pulses when the A should go to logic 1, but instead stays stuck at 0.



Fault is identified

Figure 20 - ATE A stuck at 0.

The same test was then carried out for faults of C stuck at 1, and D stuck at 0. The graphs for both tests are below. The blue cursor on the graph indicates the start of the fault condition pulsing just as C is meant to drop to logic 0 but sticks at 1, as well as doing the same when D is meant to pulse to 1 but fails to and stays stuck at 0.

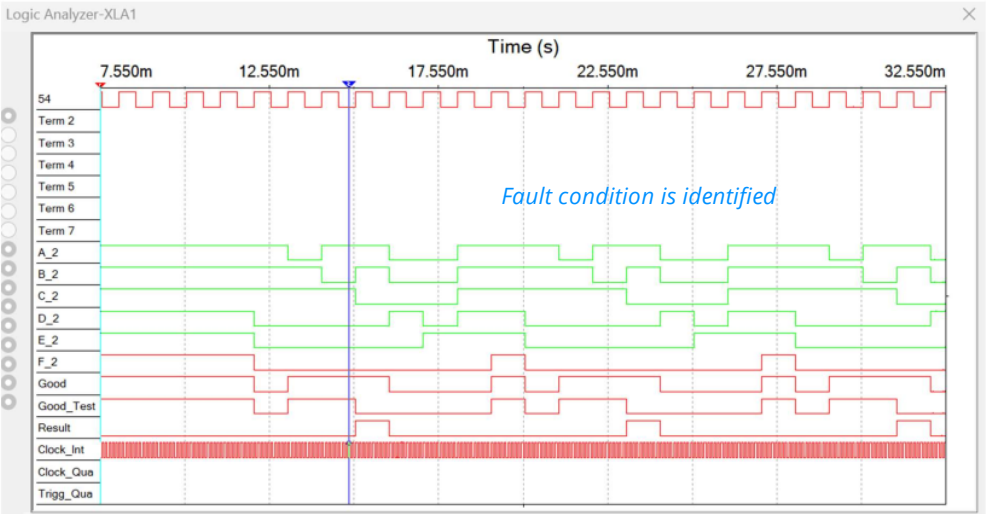


Figure 21 - ATE C stuck at 1.

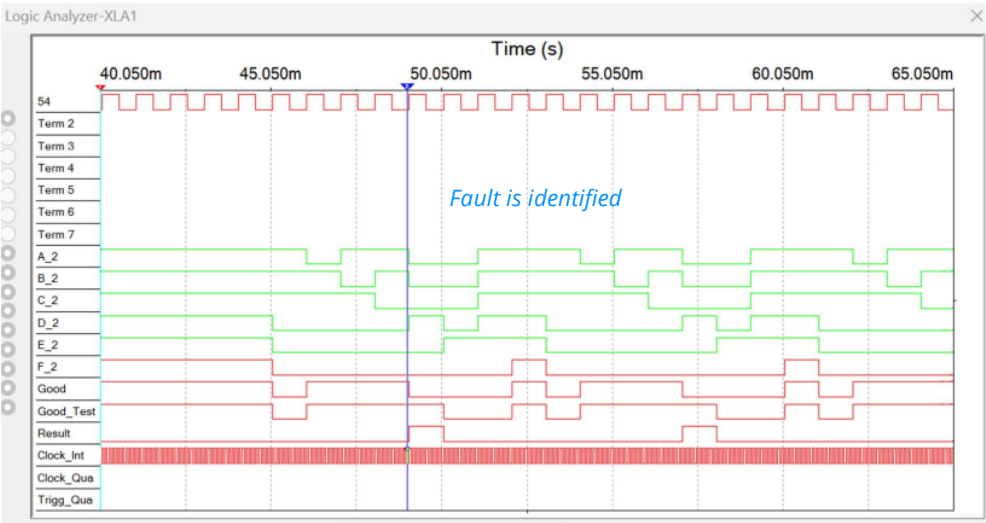


Figure 22 - ATE D stuck at 0.

This is where the LabVIEW heading belongs

The 2nd method used for testing was to build the prototype using LabView and the National Instruments ELVIS prototyping board. The images of evidence from this testing procedure can be found under section 9.2. NI LabView and NI Elvis Prototyping. The table below shows a comparison of results from both tests carried out and they were both a success as they produced the same results, as expected.

	Multisim 6 Bit Register				LabView and ELVIS Prototype			
	No Fault	A SA0	C SA1	D SA0	No Fault	A SA0	C SA1	D SA0
Fault Detected	NO	YES	YES	YES	NO	YES	YES	YES

Table 5 - 2 types of prototype results

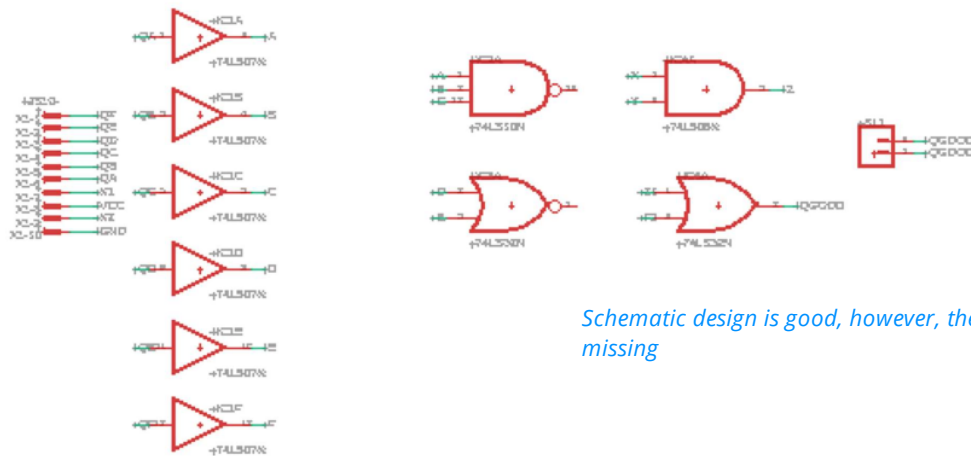
Good use of table

The LabVIEW G-code design and explanation should be here

PCB prototype test section is missing

6. CAM design and build of prototype.

The Computer Aided Manufacture (CAM) software used to develop the double-sided sustainable prototype PCB was called Eagle, by Autodesk. This was used to draw the schematic, which was then converted to a Gerber file so that it could be converted into a PCB design. The schematic can be seen below.



Schematic design is good, however, the PCB design is missing

Figure 23 - Eagle schematic

The Gerber files generated from Eagle software were transferred to a company called PCBWay, where the PCB was developed and printed. These gerber files can be seen in appendix section 9.3. CAM Design of Prototype. This process of manufacturing the PCB meets the needs of a customer as it was physically tested with a prototype, as carried out during the assignment, therefore it was manufactured reliably, and sustainably by using recyclable components which have been produced ethically and legally.

Good points made about the Gerber files

7. Conclusions and Recommendations

This assignment provided the author with solid background knowledge from carrying out the research task into topics such as fault modelling on IC's, the manufacturing advantages and drawbacks, modern techniques of sustainable manufacturing using vision systems, and the effects of electro-static discharge and the methods used to prevent it.

This knowledge was put into practice throughout the assignment, as the stuck at fault modelling was used extensively during the design and construction of the PCB CUT to ensure the IC was manufactured successfully. The stuck at fault modelling was used during the design process using truth tables, then put into practice via a simulation process using Multisim and then also practically by using an NI Elvis board to build a prototype. This was proven in the comparison Table 5. All these tests were carried out successfully, which lead to the circuit being exported to gerber files before being printed out as an IC via the company PCBWay. This proved the theory to be correct, as the results provided the exact results as expected, which confirmed the correct operation of the CUT. *The ECAD and practical are identified as separate here, and therefore should have separate headings in the report*

From the research carried out into ATE design and production, a major factor to consider during this manufacturing process is ESD. This is a potentially high dangerous scenario where humans and equipment can get severely damaged if not protected sufficiently. Therefore, to conclude the research, it should be ensured that all workers wear grounding wristbands when working on the PCB's, as well as having grounding mats installed around the factory. The packaging should also be static free.

The test methods provided a good overall performance, with results that were easily tabulated to compare against each other and to confirm correct operation. It is essential that during IC fabrication that correct testing gets carried out, however depending on how it is carried out it can be costly. The methods used during this assignment were inexpensive and provided sufficient results for the circuits required by the customer. If a circuit was highly complex and it was essential for it to be tested rigorously, a bed of nails tester would potentially be a better option for testing. However, in this assignment the Multisim and LabView software was sufficient, as well as the physical prototyping before the PCB was produced.

A good relevant recommendation

A reasonable conclusion. The prototype PCB is missing from the report and conclusion,however, relevant recommendations are included.

8. Citation List

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A good number of sources used in the research

9. Appendix

9.1. Karnaugh maps

ABC DEF	000	001	011	010	100	101	111	110
000	0	0	1	0	0	1	0	0
001	0	0	0	0	0	0	0	0
011	0	0	0	0	0	0	0	0
010	1	0	0	0	0	0	0	0
100	0	0	0	0	0	0	0	0
101	0	0	0	0	0	0	0	0
111	0	0	0	0	0	0	1	0
110	0	0	0	0	0	0	1	0

Table 6 - Output QA

ABC DEF	000	001	011	010	100	101	111	110
000	0	0	0	0	0	1	1	0
001	0	0	0	0	0	0	0	0
011	0	0	0	0	0	0	0	0
010	1	0	0	0	0	0	0	0
100	0	0	0	0	0	0	0	0
101	0	0	0	0	0	0	0	0
111	0	0	0	0	0	0	1	0
110	0	0	0	0	0	0	1	0

Table 7 - Output QB

ABC DEF	000	001	011	010	100	101	111	110
000	0	0	1	0	0	0	1	0
001	0	0	0	0	0	0	0	0
011	0	0	0	0	0	0	0	0
010	1	0	0	0	0	0	0	0
100	0	0	0	0	0	0	0	0
101	0	0	0	0	0	0	0	0
111	0	0	0	0	0	0	1	0
110	0	0	0	0	0	0	1	0

Table 8 - Output QC

ABC DEF	000	001	011	010	100	101	111	110
000	0	0	0	0	0	0	0	1
001	0	0	0	0	0	0	0	0
011	0	0	0	0	0	0	0	0
010	1	0	0	0	0	0	0	0
100	0	0	0	0	0	0	0	0
101	0	0	0	0	0	0	0	0
111	0	0	0	0	0	0	0	0
110	0	0	0	0	0	0	1	0

Table 9 - Output QD

ABC DEF	000	001	011	010	100	101	111	110
000	0	0	0	0	0	0	0	0
001	0	0	0	0	0	0	0	0
011	0	0	0	0	0	0	0	0
010	1	0	0	0	0	0	0	0
100	1	0	0	0	0	0	0	0
101	0	0	0	0	0	0	0	0
111	0	0	0	0	0	0	0	0
110	0	0	0	0	0	0	1	0

Table 10 - Output QE

ABC DEF	000	001	011	010	100	101	111	110
000	0	0	0	0	0	0	0	0
001	0	0	0	0	0	0	0	0
011	0	0	0	0	0	0	0	0
010	0	0	0	0	0	0	0	0
100	0	0	0	0	0	0	0	0
101	0	0	0	0	0	0	0	0
111	0	0	0	0	0	0	0	0
110	0	0	0	0	0	0	1	0

Table 11 - Output QF

K-maps are correct and ref from main report

9.2. NI LabView and NI Elvis Prototyping

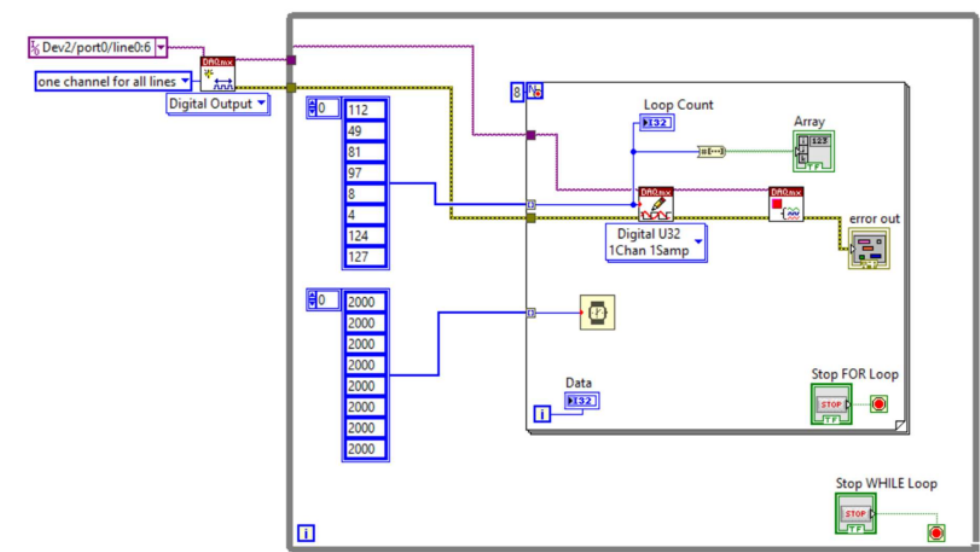


Figure 24 - NI LabView Block Diagram

This code needs some explanation and would be better situated in the implementation and design sections of the report

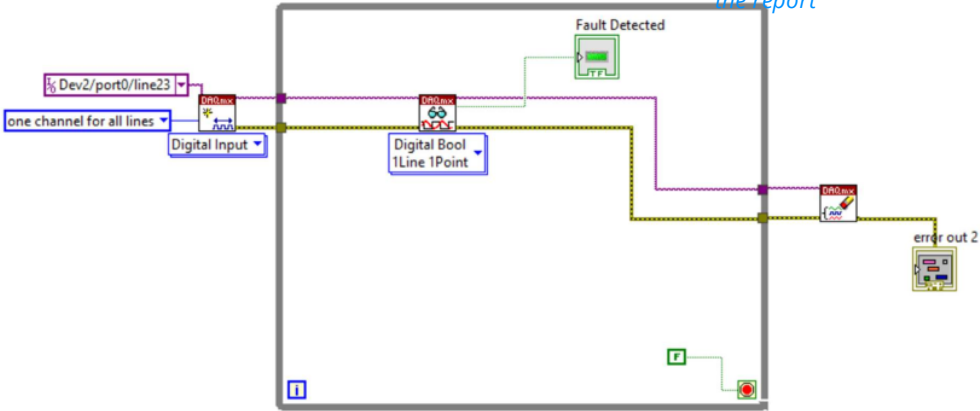


Figure 25 - NI LabView Block Diagram_1

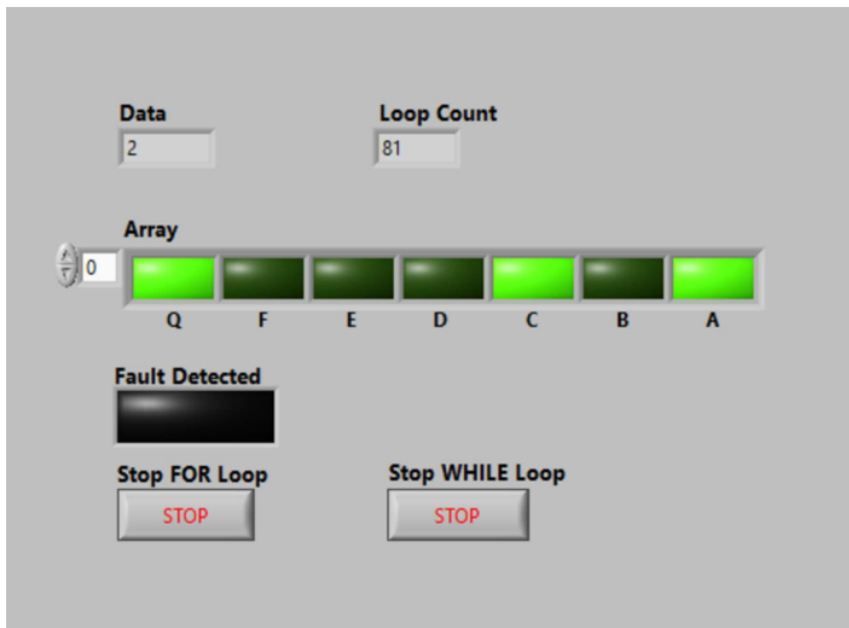


Figure 26 - LabView No Fault Found

NFF condition is identified

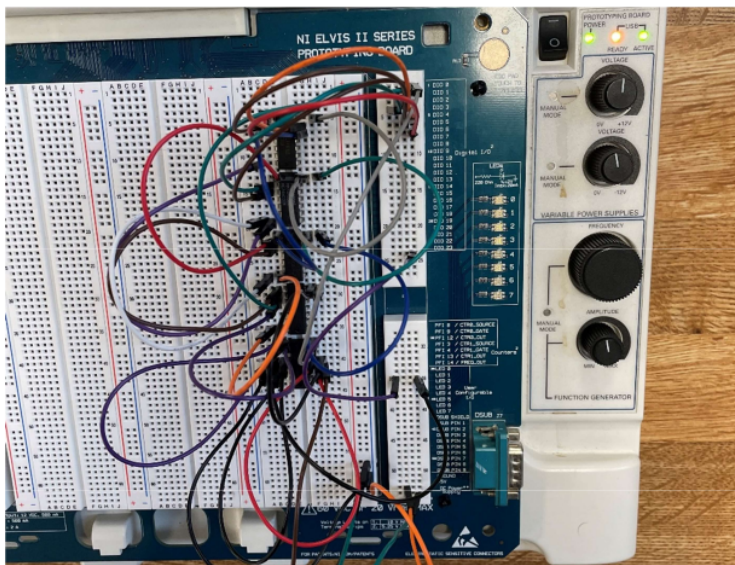


Figure 27 - ELVIS No Fault Found

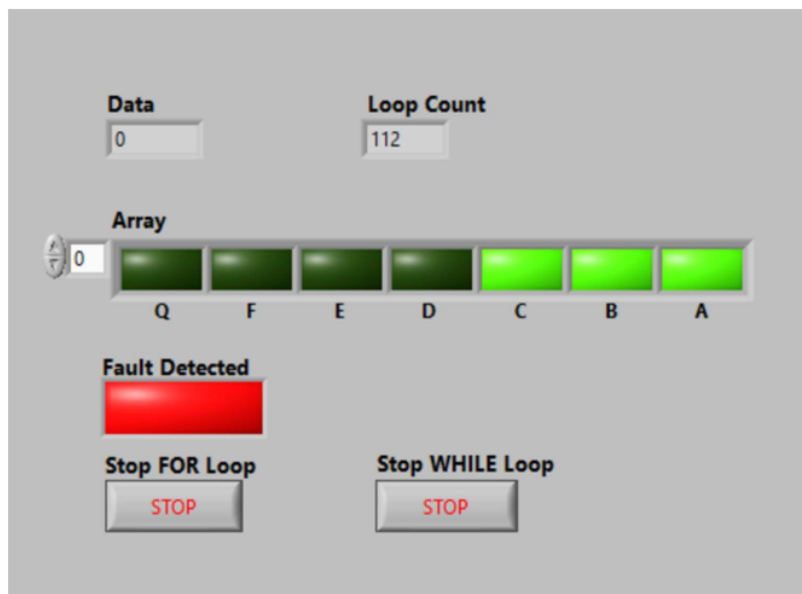


Figure 28 - LabView A stuck at 0.

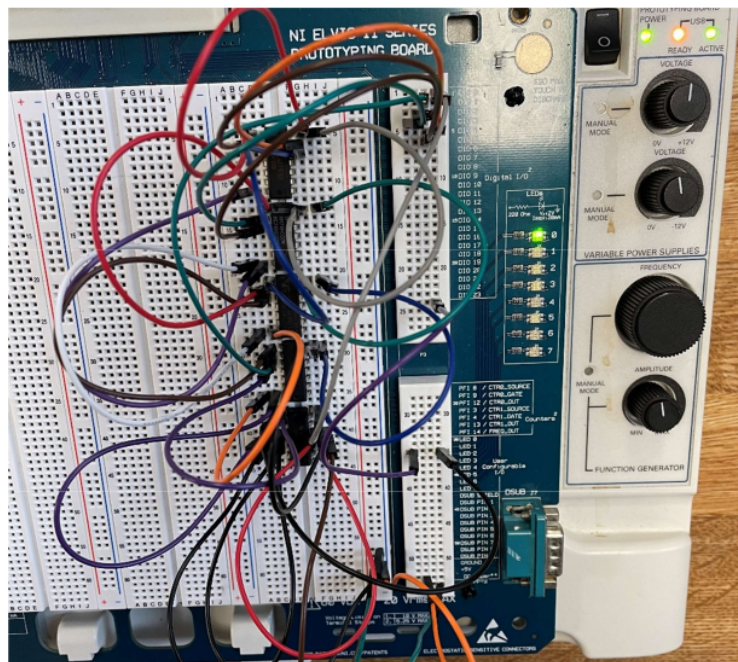


Figure 29 - ELVIS A stuck at 0.

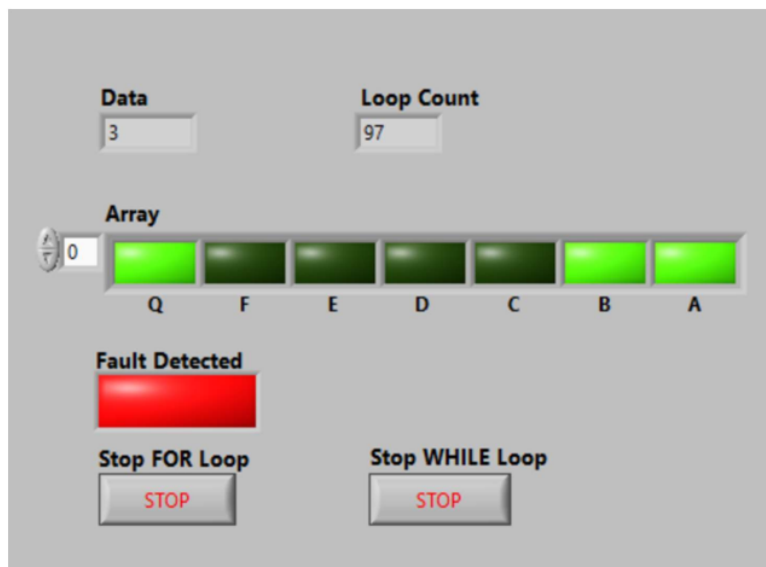


Figure 30 - LabView C stuck at 1.

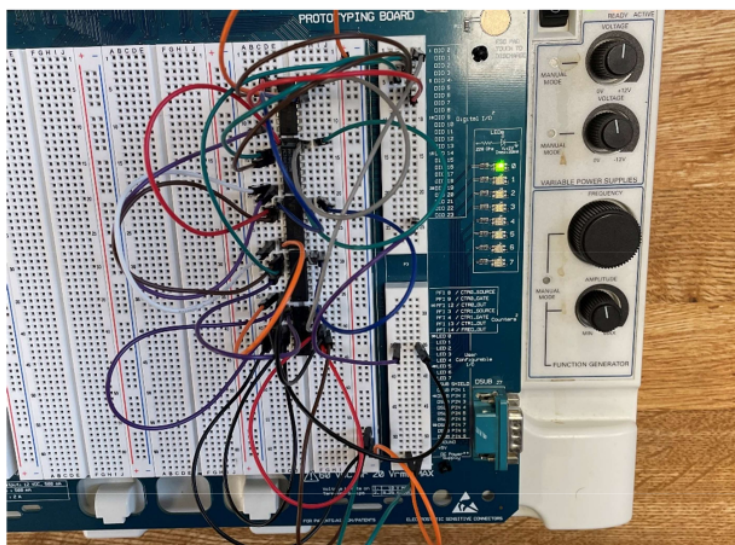


Figure 31 - ELVIS C stuck at 1.

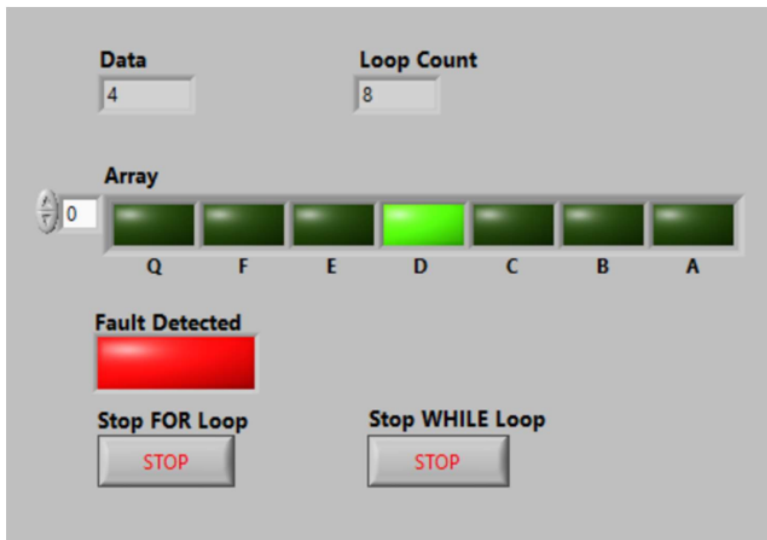


Figure 32 - LabView D stuck at 0.

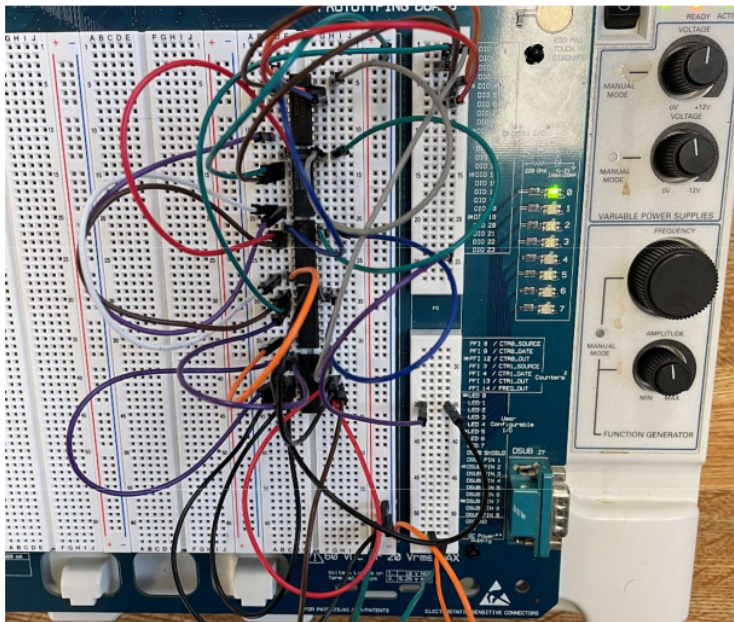


Figure 33 - ELVIS D stuck at 0.

The three fault conditions have been tested with fault condition indicated

The PCB prototype tests are missing

9.3. CAM Design of Prototype

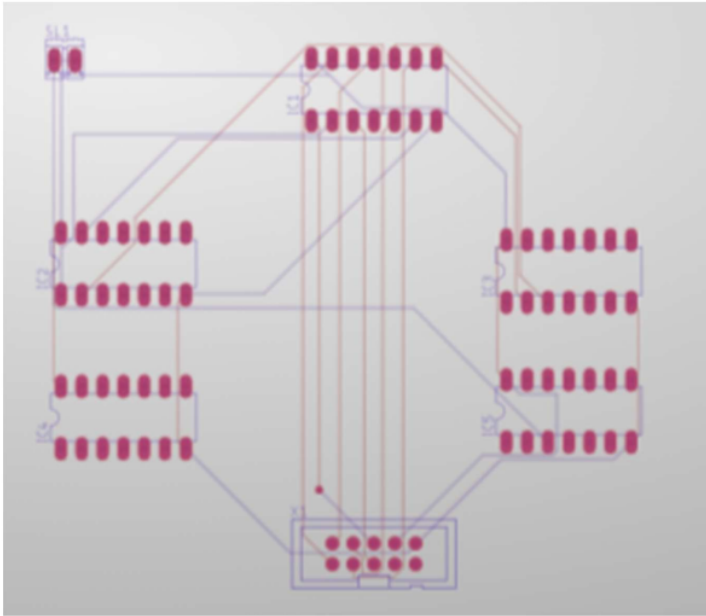


Figure 34 - Gerber all layers on

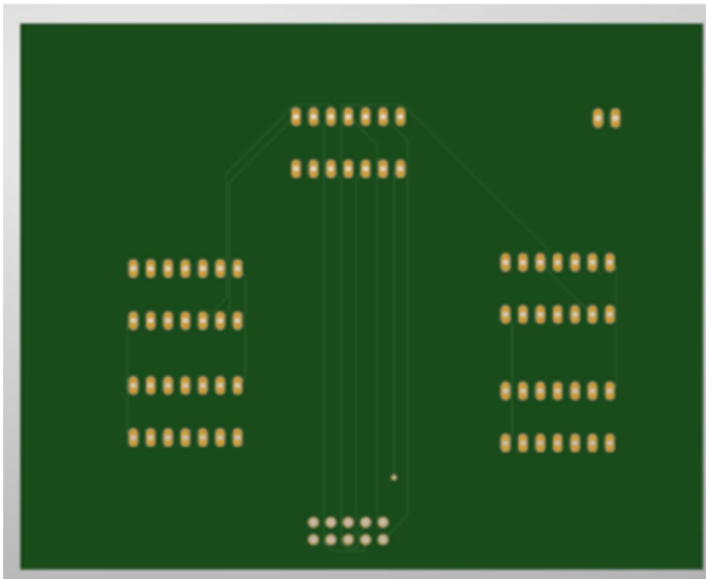


Figure 35 - Gerber bottom view

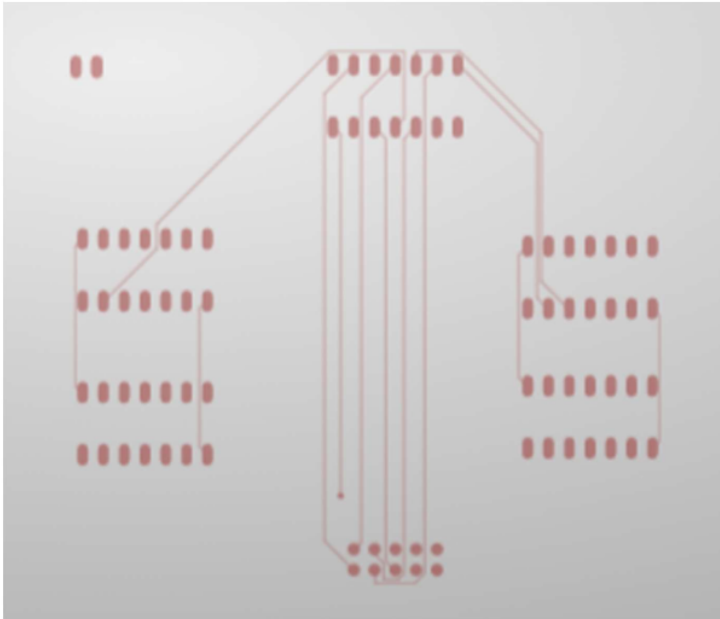


Figure 36 - Gerber copper bottom layer



Figure 37 - Gerber mechanical drill layer

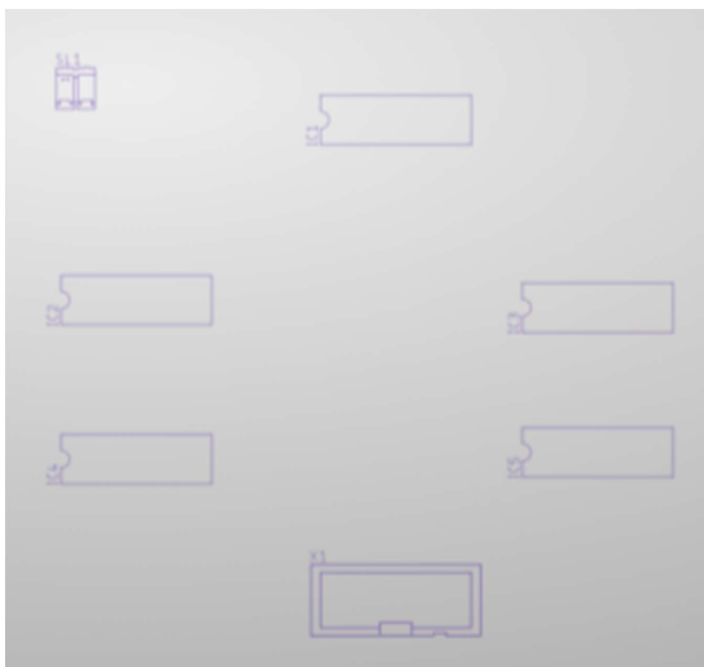


Figure 38 - Gerber silkscreen top layer



Figure 39 - Gerber soldermask bottom layer



Figure 40 - Gerber soldermask top layer

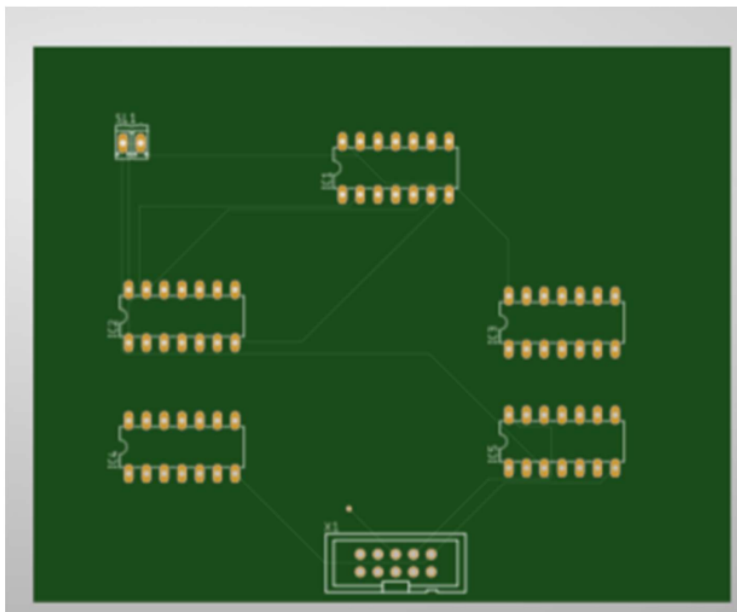


Figure 41 - Gerber top view

FINAL GRADE

GENERAL COMMENTS

Instructor

61 / 100

PAGE 1

PAGE 2

PAGE 3

Text Comment. Good extensive list of figures

Text Comment. Good list of tables

PAGE 4

Text Comment. Good organised table of contents

PAGE 5

Text Comment. Summary could be more detailed for the same word count

PAGE 6

Text Comment. Good explanation with supporting images

PAGE 7

Text Comment. Good research on different types of SSF

PAGE 8

Text Comment. Good research on ESD and preventive measures. Application examples could have been included to support the preventive measures research

PAGE 9

Text Comment. Good points identified with relevant source

Text Comment. There are wider areas to investigate here, such as frequency signature recognition which is becoming popular with contactless sensing topic areas.

PAGE 10

PAGE 11

Text Comment. Good redundancy methods used for each logic gate

PAGE 12

Text Comment. Table has been created from the theory of SSF modelling

Text Comment. Significant key rule is identified here.

PAGE 13

Text Comment. Good reduction methods used by applying the wildcard rule to further reduce the number of test vectors.

PAGE 14

Text Comment. Good use of ECAD alternative functions for ATE development. This demonstrates a good understanding of requirements

Text Comment. NFF condition is identified. This is a critical state to achieve before testing can be carried out.

PAGE 15

Text Comment. Good fault indicator

Text Comment. Fault condition has been identified

PAGE 16

Text Comment. Do not use this word. Alternative words are: altered, changed or reconfigured.

Text Comment. Fault is identified correctly

PAGE 17

Text Comment. Fault condition evidence and associated test results have been explained.

PAGE 18

Text Comment. This section is not using LabVIEW

Text Comment. Next state table is correct

PAGE 19

Text Comment. Good identification of X-OR function

PAGE 20

Text Comment. NFF condition is achieved. Critical before carrying out further tests

Text Comment. Fault is identified

PAGE 21

Text Comment. Fault condition is identified

Text Comment. Fault is identified

PAGE 22

Text Comment. This is where the LabVIEW heading belongs

Text Comment. Good use of table

Text Comment. The LabVIEW G-code design and explanation should be here

Text Comment. PCB prototype test section is missing

PAGE 23

Text Comment. Schematic design is good, however, the PCB design is missing

Text Comment. Good points made about the Gerber files

PAGE 24

Text Comment. The ECAD and practical are identified as separate here, and therefore should have separate headings in the report.

Text Comment. A good relevant recommendation

Text Comment. A reasonable conclusion. The prototype PCB is missing from the report and conclusion, however, relevant recommendations are included.

PAGE 25

PAGE 26

Text Comment. A good number of sources used in the research

PAGE 27

PAGE 28

PAGE 29

Text Comment. K-maps are correct and ref from main report

PAGE 30

Text Comment. This code needs some explanation and would be better situated in the implementation and design sections of the report

PAGE 31

Text Comment. NFF condition is identified

PAGE 32

PAGE 33

PAGE 34

Text Comment. The three fault conditions have been tested with fault condition indicated

Text Comment. The PCB prototype tests are missing

GRADING FORM: CSG-RUBIC

MATTHEW DAVIES**0****RESEARCH-INFORMED LITERATURE**



Research has many significant point covered, however there could be more coverage on contactless testing such as using frequencies. There are a good number of relevant sources used in the research.

14/20**KNOWLEDGE AND UNDERSTANDING**



A good understanding has been demonstrated in creating the test vectors from the theoretical principles. However there are parts missing for the prototype, including the testing. 3/5 LabVIEW design demonstrates a good knowledge of system development and the funtions required to run the test vextors. The code functions should have been explained. 3/5 ECAD alternative ATE methods ahve been designed using alternative functions to meet the requirements. 3.5/5 CAM design and

12/20

development demonstrates a n understanding, however, the PCB CAM is missing from the report. This should be included and explained. 2.5/5

ANALYSIS

 ECAD analysis is covered and explained enough to demonstrate a good understanding. 7.5/10 Tests carried out follow the theory. 3.5/5 Conclusion covers significant points and includes good relevant recommendations. However the prototype PCB was not in the report and therefore not in the conclusion. 3/5

14/20

PRACTICAL APPLICATION AND DEP.

 Only the first part of the prototype is included in the report. The PCB section with LabVIEW (implementation and test) is missing. 4/10 The final prototype test with LabVIEW is missing. 4/10

8/20

SKILLS FOR PROFESSIONAL PRAC.

 Extensive use of relevant software is evident in the report. 6.5/10 Report layout is good, however there are parts in the wrong places and parts missing. 3/5 Word count is within limits and good use of appendices. 3.5/5

13/20