

ASTABLE 555 TIMER CIRCUIT

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INTRODUCTION

This report details the simulation and testing of timer circuit utilizing a 555 Timer Integrated Circuit (IC). The 555 IC was the first commercially available IC, introduced in 1971 by the Signetics Corporation [1]. It is widely available, cost-effective (£0.42 each [2]), and can operate in three multivibrator operation modes: monostable, bistable and astable. The 'multivibrator' refers to the circuit's output consisting of 2-states, ON and OFF. 'Monostable' mode, also referred to as 'one-shot' mode produces a single output pulse of fixed time upon triggering; 'Bistable' mode, also referred to as 'latch' mode, produces an output pulse upon triggering until a second trigger input; and 'Astable' mode, also referred to as 'oscillator' mode, which has been used for the purposes of this report, in which the output oscillates between the 2 states continuously, generating an 'ON/OFF' cyclical square wave output [3].

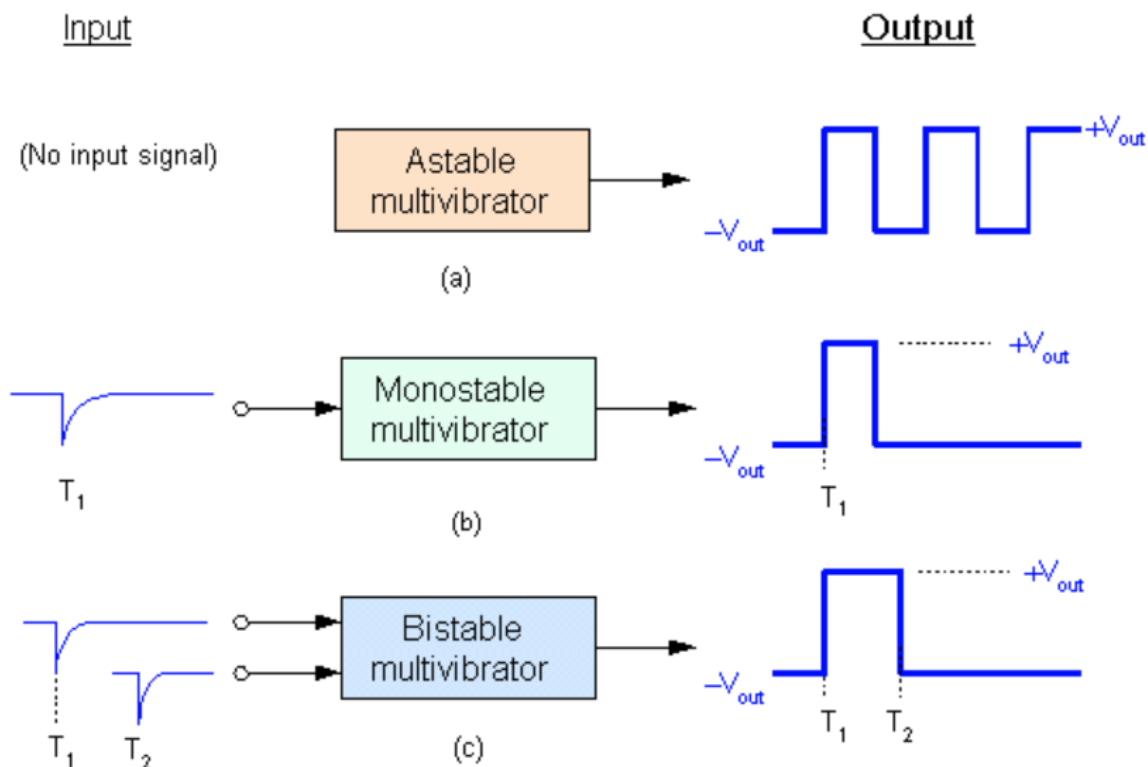


FIGURE 1 - WAVEFORM EXAMPLES OF THE THREE 555 TIMER IC MULTIVIBRATION MODES [4]

The output pulse duration and voltage of the 555 IC can be modulated by the use of external resistors and capacitors to produce pulse times ranging from microseconds to hours [5]. The 555 IC has vast potential applications, from simple LED blinking circuits as has been used in this report, to an easily configurable waveform generator. Astable circuits can also be used as a reference to detect 'missing' signals on more complex circuits.

CIRCUIT DIAGRAM

A circuit diagram was supplied, shown in Figure 2. Resistor 3 and 4 (R3 and R4, respectively) were determined by available components.

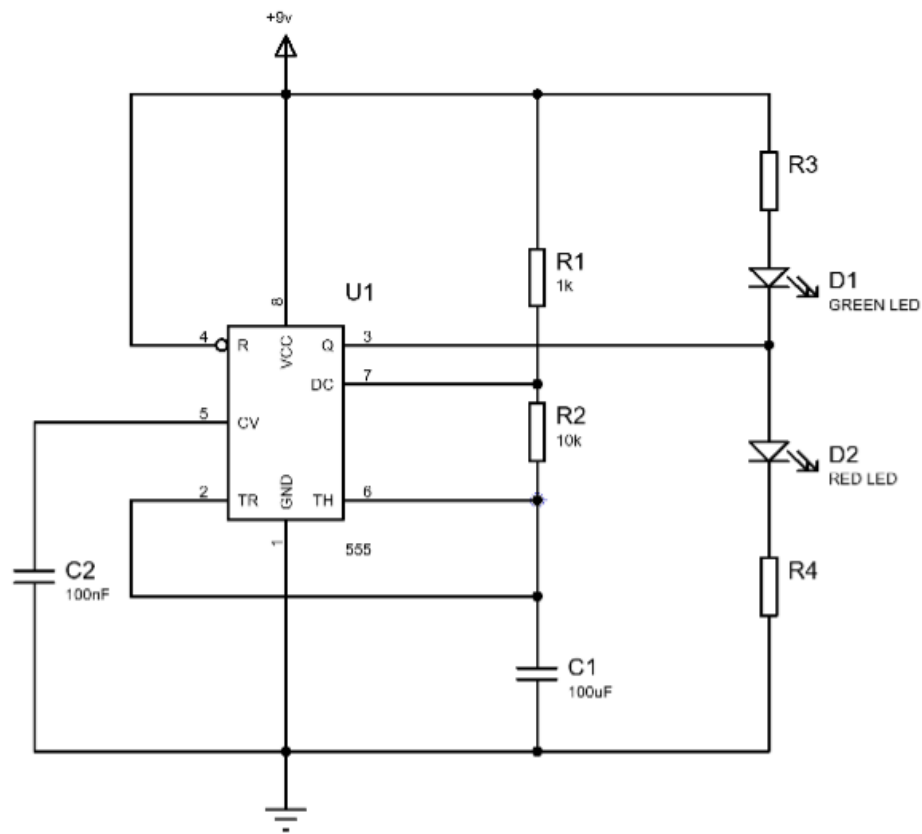


FIGURE 2 - GIVEN 555 TIMER CIRCUIT DIAGRAM FROM ASSIGNMENT BRIEF

SIMULATION

The circuit was simulated in Proteus, as may be seen in Figure 3. Proteus enables the use of a digital oscilloscope; seen in Figure 4, to measure the amplitude (Voltage) and time of signal at various points within the simulated circuit.

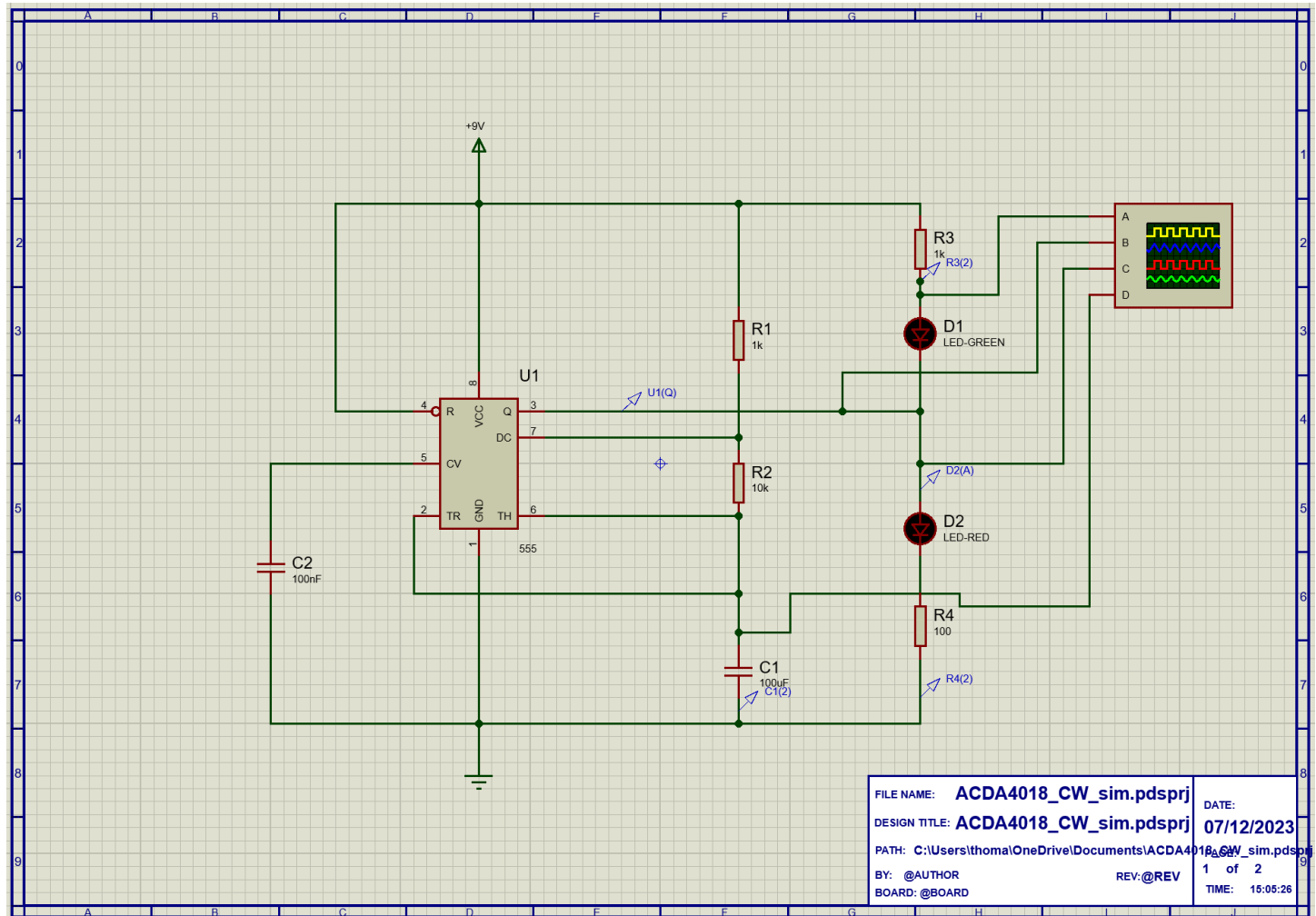


FIGURE 3 - SIMULATED CIRCUIT IN PROTEUS

DESIGN VALUES

To determine the output pulse timing of the circuit, digital 'probes' are placed at resistor R3 for channel A, at the IC output pin Q for channel B, between Q and D2 for channel C, and finally at C1 for channel D. The channel C probe was later moved to after D2 to measure the voltage drop across the LED (Figure 6). The results of the digital oscilloscope can be seen in Figure 4 below.

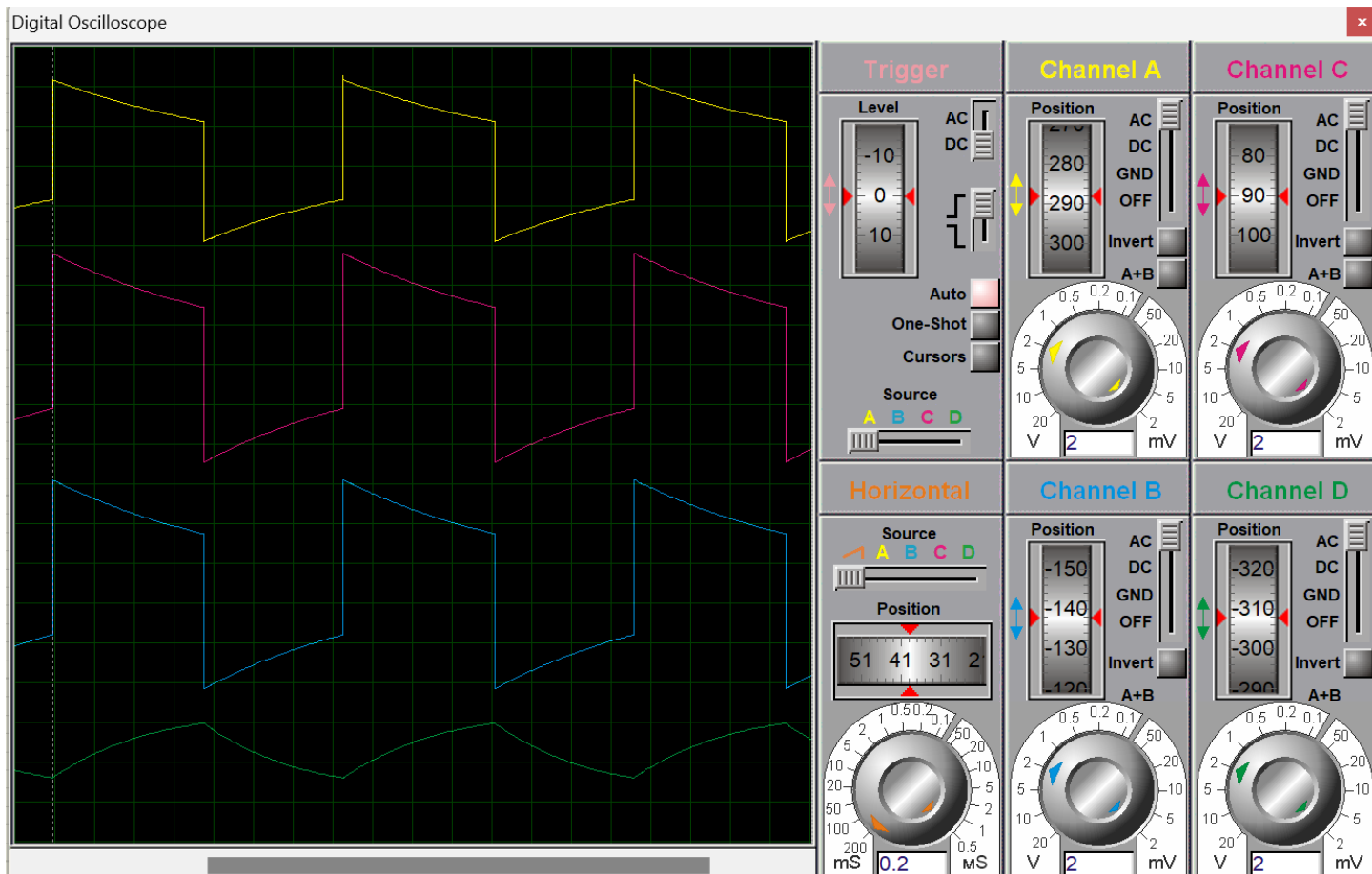


FIGURE 4 - DIGITAL OSCILLOSCOPE READ OUT FROM SIMULATED CIRCUIT

Timing markers are placed on the waveform maximum and minimum voltage of channel B (Output Q [pin 3] of the 555 IC) as seen in Figure 5Figure 4 with results in

Table 1.

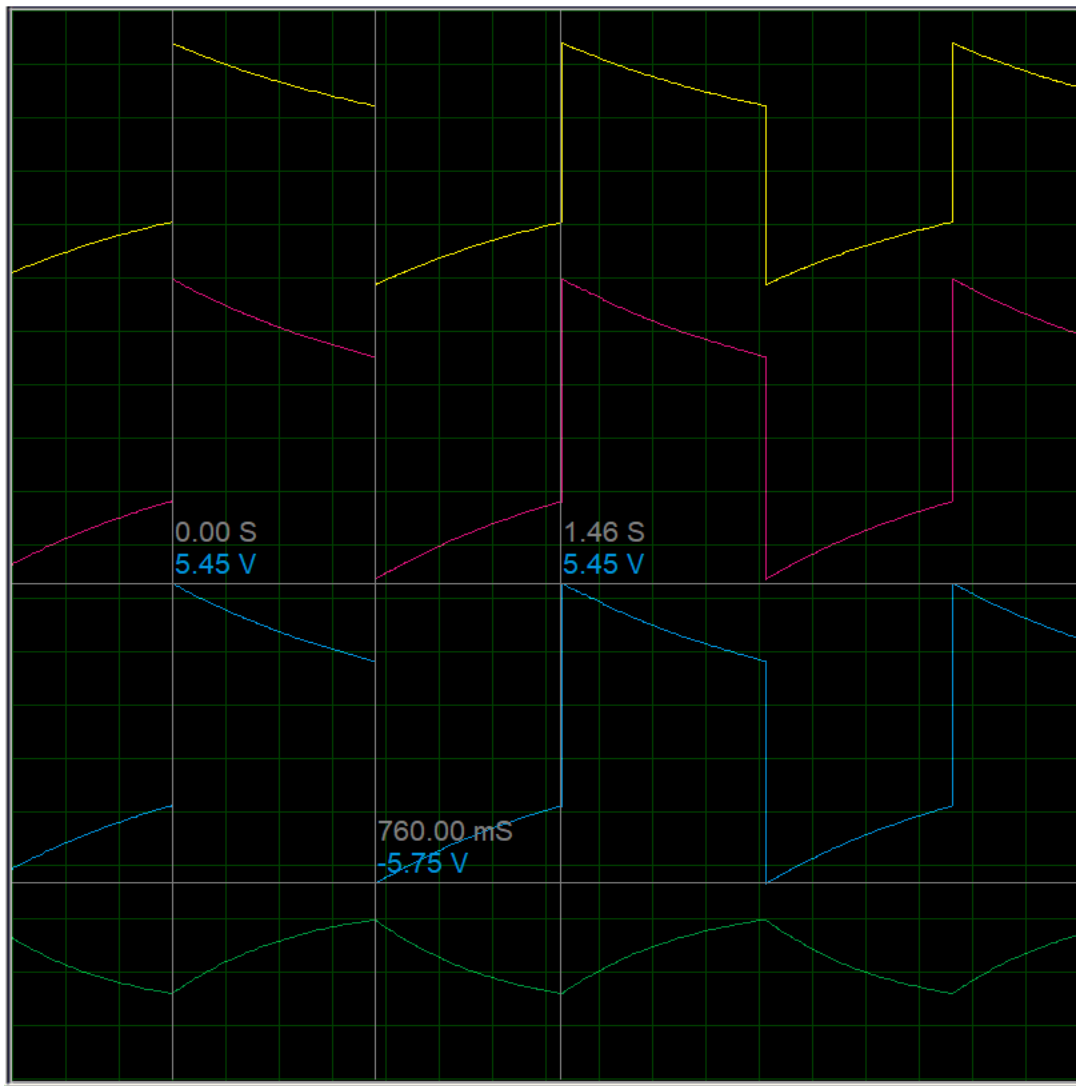


FIGURE 5 - TIMING MARKERS ON Q OUTPUT

Time period [T]	Time [s]	Voltage [V]	C1 [V]
T = 0	0.00	5.45	1.35
$\frac{1}{2} T$	0.760	-5.75	-1.5
T	1.46	5.45	1.35

TABLE 1 – SIMULATED CIRCUIT VALUES

For output pin Q, the pulse is in an 'ON' state from $T = 0$ to $\frac{1}{2}T$ is the 'ON' time of the pulse. The pulse is then in an 'OFF' state from $\frac{1}{2}T$ to T is the 'OFF' time. The frequency of the pulse can then be calculated from the value of T , using the following equation: $f = \frac{1}{T} = \frac{1}{1.46S} = 0.685\text{kHz}$. The total amplitude of the pulse is equal to the difference in voltage measured at $T = 0$ and at $\frac{1}{2}T$. Using the values obtained in the present simulation, the total amplitude of the pulse is calculated as $11.2V$. The capacitor C1 charges to a maximum voltage of $1.35V$ and a minimum of $-1.5V$, giving a total amplitude of $2.85V$.

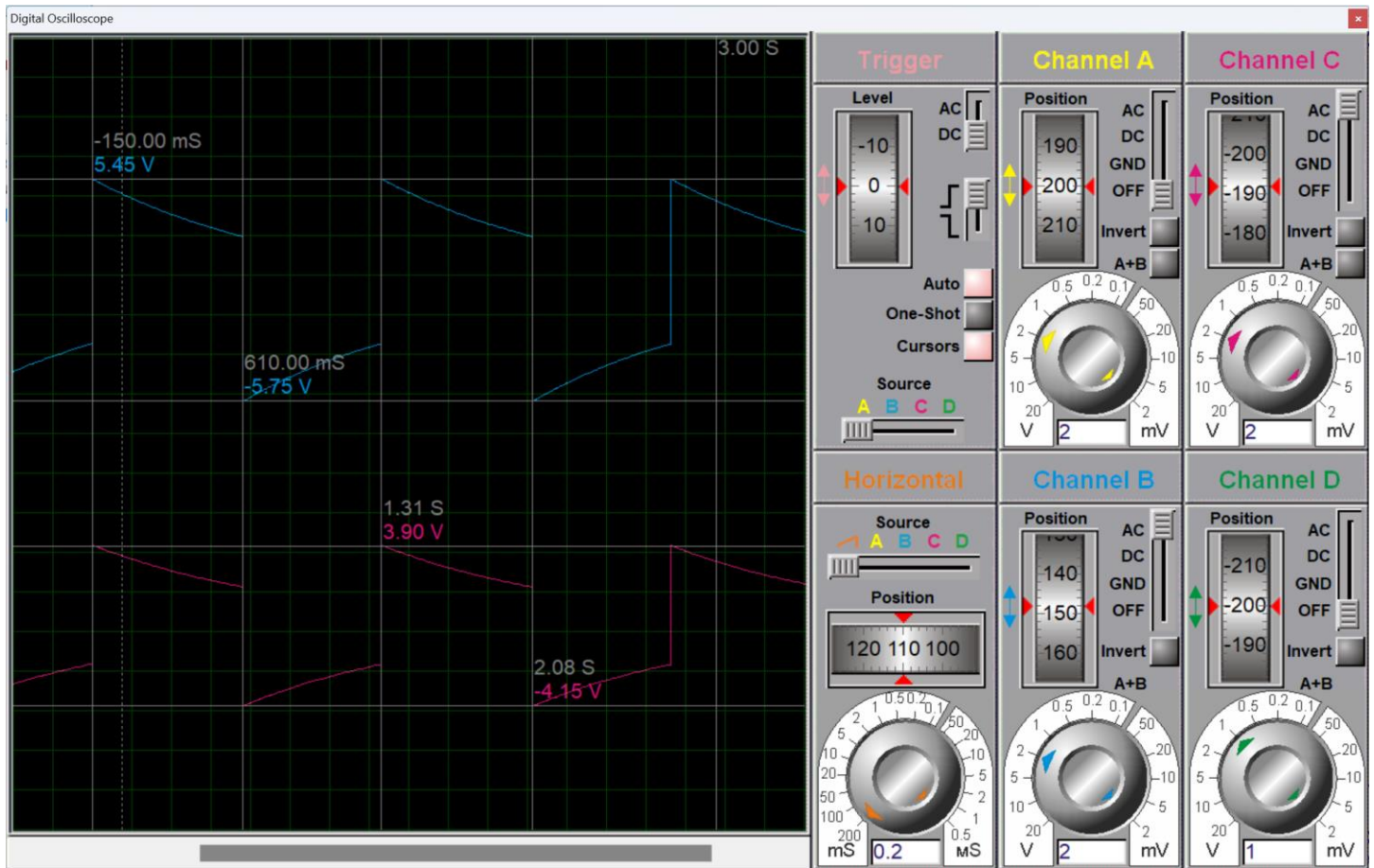


FIGURE 6 - PROBES ON Q AND AFTER D2 TO MEASURE THE VOLTAGE DROP ACROSS THE LED

The voltage drop across D2 is measured to be 1.55V from the maximum voltages of the 'ON' pulses from output Q and D2 (Figure 6).

BREAD BOARD

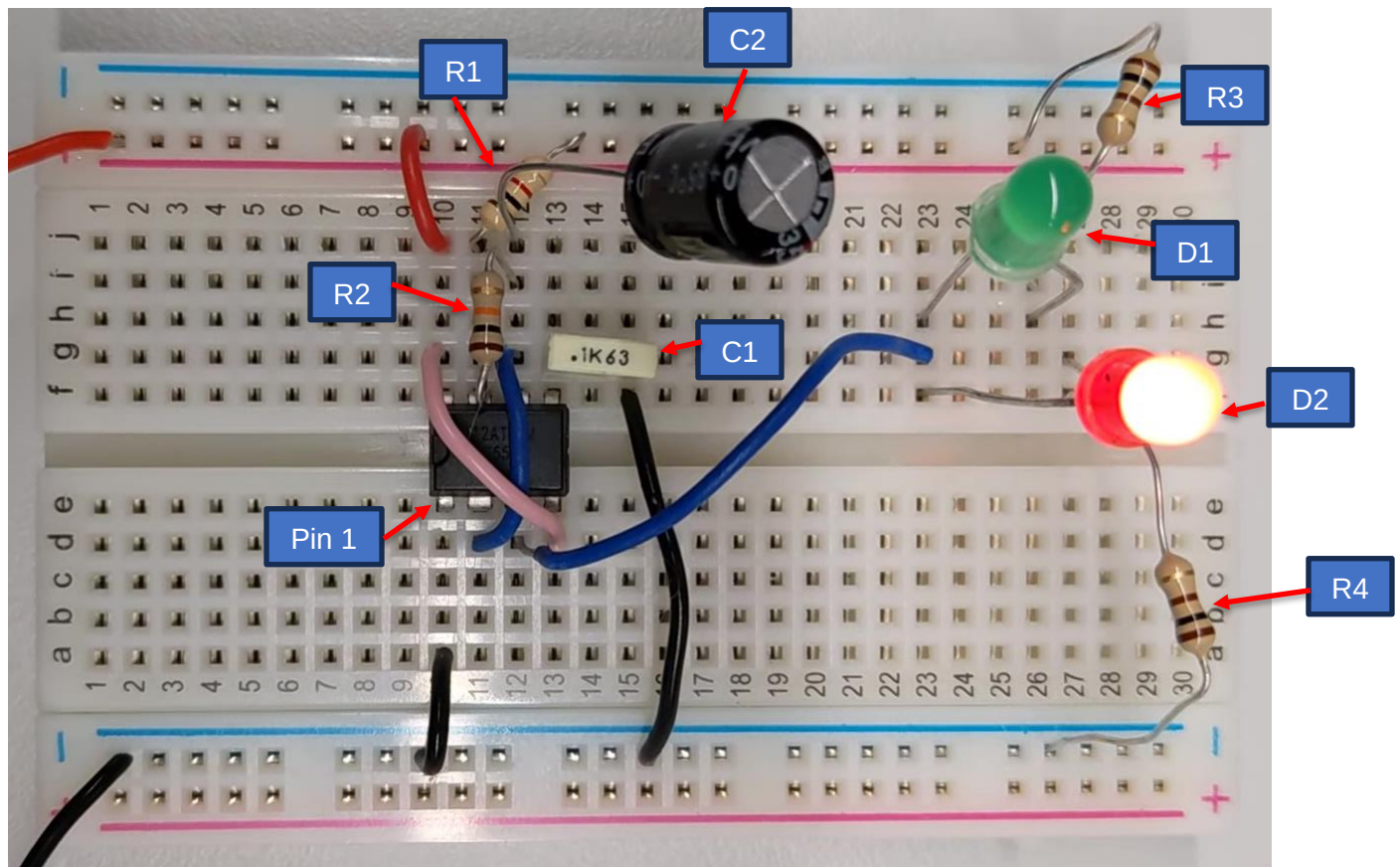


FIGURE 7 - BREADBOARD CIRCUIT

Figure 7 shows the breadboard circuit that was tested. The breadboard circuit was connected to reflect the circuit diagram shown in Figure 2. The dimple on the 555 timer IC indicates the top is on the left hand side and therefore the pins run from 8 to 5 on the top row and 1 to 4 on the bottom row (left to right). The top power rail was connected to a DC bench-top power supply set to 9V, this supply voltage is connected to J10 which is in series with pin 8 (VCC) of the chip. The bottom power rail is connected to the negative terminal of the supply to provide a reference voltage of 0V which is connected in series by A10 to pin 1 (GND).

Pin 2 (TRIG) is bridged to pin 6 (THRS). Pin 2 triggers the timer when a voltage of 1/3rds supply is supplied and pin 6 resets the internal comparator at 2/3rds supply voltage. These voltages are supplied by C1 and C2 and are in series with R2 and therefore pin 7 (DISCH) which triggers the capacitors to discharge.

Pin 4 (RESET) is bridged to the supply voltage to put the chip into astable mode. A constant 9V is supplied and therefore a reset signal to stop the timer of 1/3rds supply voltage is not possible.

Pin 3 (OUT) provides the output pulse to the Light Emitting Diodes (LEDs) D1 and D2. The cathode of D1 is connected in series to the voltage supply via R3 and the anode to pin 3; as such when there is no output voltage from pin 3, D1 will light up. When there is an output voltage D1 will be reverse biased and will not emit light. The cathode of D2 is connected in series to pin 2 and is therefore forward biased, and consequently emits light when there is a output voltage as it is forward biased. This is the mechanism by which the LEDs flash alternatively with the ON OFF pulse of the 555 timer IC.

BREAD BOARD VALUES

Figure 8 shows the connection of oscilloscope probes to the output pin 2 of the IC and to the cathode of C2 to measure the output pulse of the timer circuit and charging cycle of C2. A probe to C1 was not possible as the capacitor is a surface mount design.

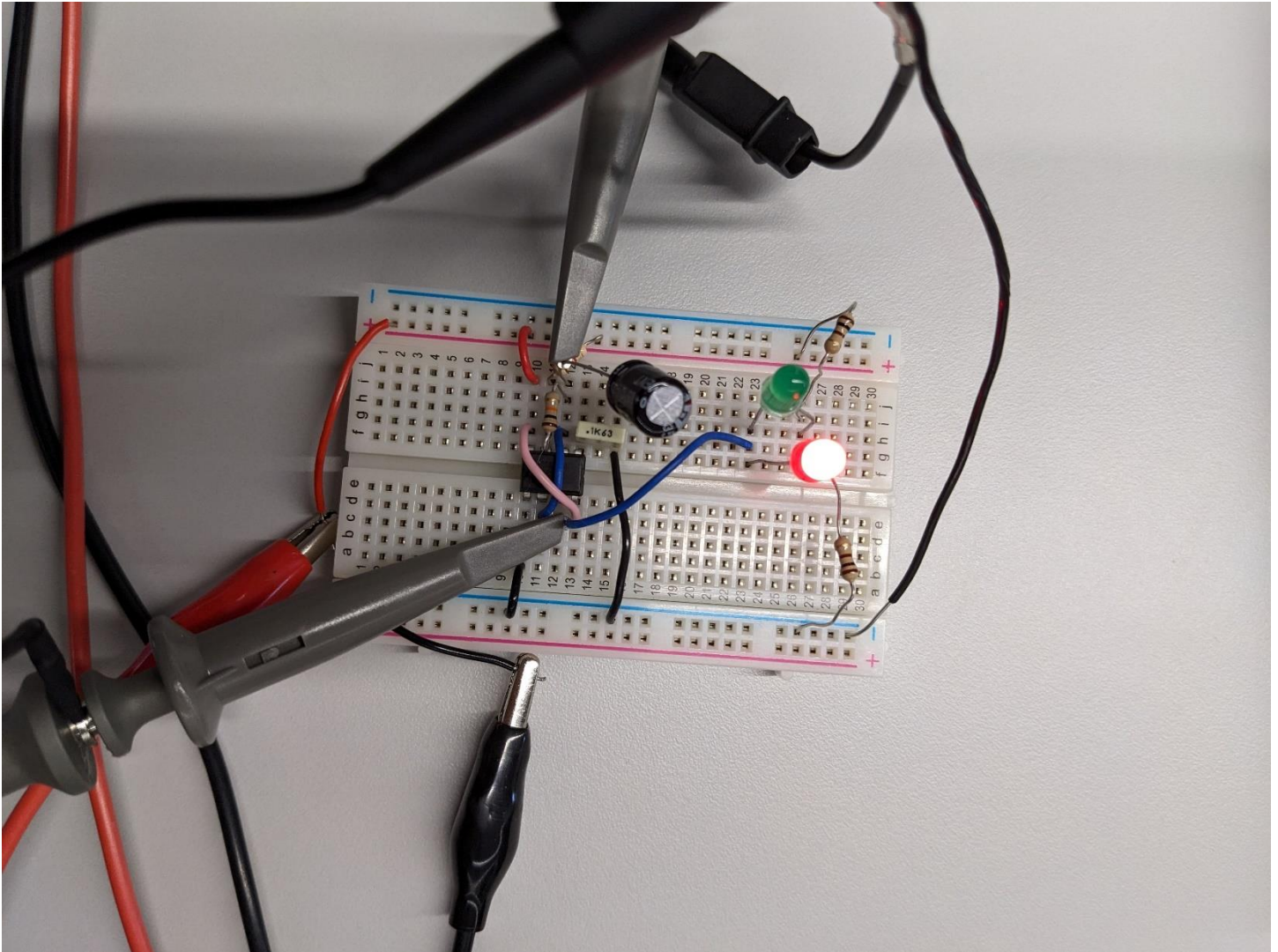


FIGURE 8 - CONNECTION OF OSCILLOSCOPE PROBES TO PIN 3 AND C2

THE READOUT OBTAINED USING THE CONNECTIONS SHOWN IN FIGURE 8 IS SHOWN IN FIGURE 9 BELOW. A TABLE OF VALUES OBTAINED FROM THAT READOUT CAN BE FURTHER FOUND IN

TABLE 2.

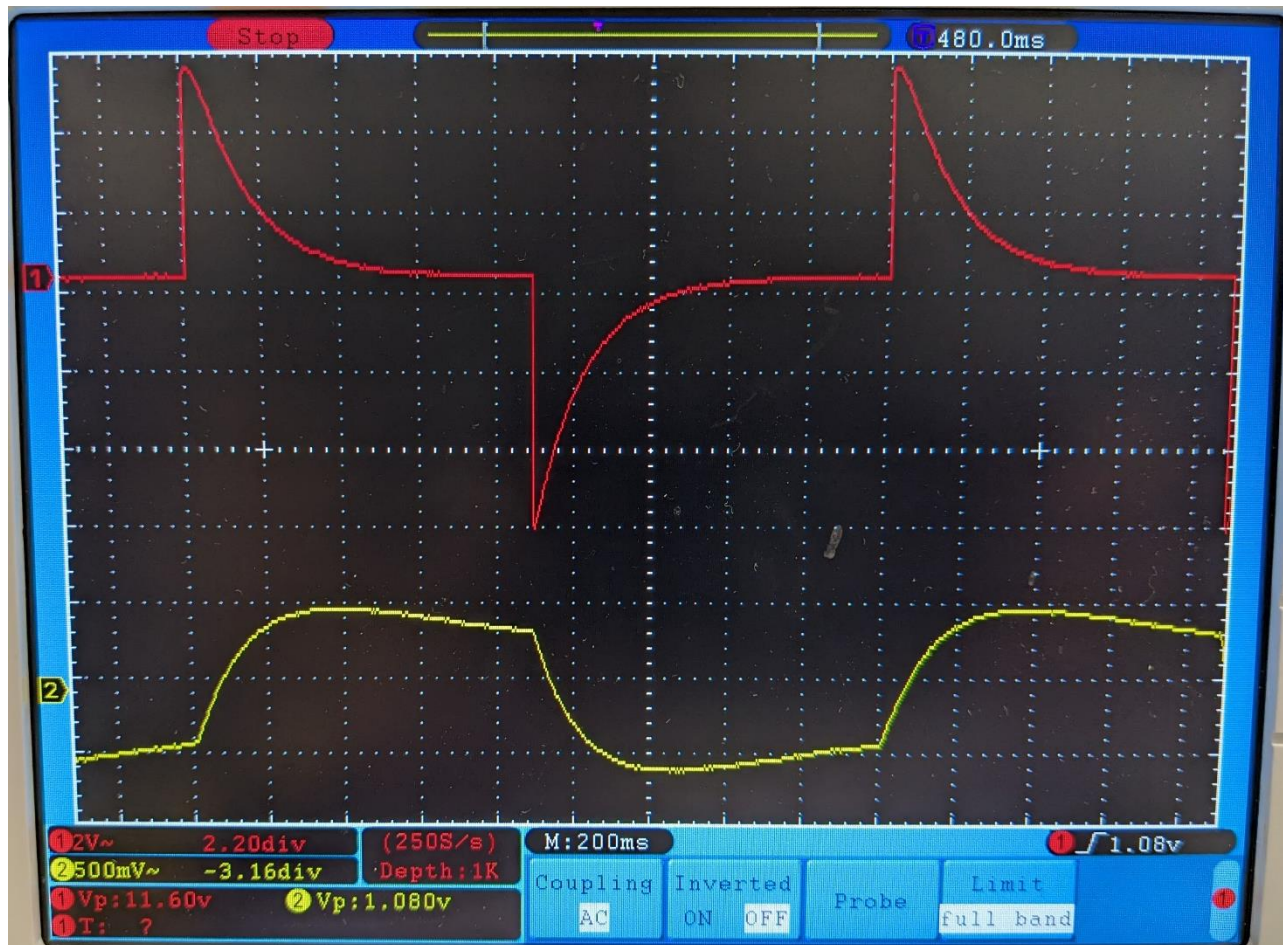


FIGURE 9 - OSCILLOSCOPE READINGS FROM PIN 2 (CHANNEL 1 - RED) AND C2 (CHANNEL 2 - YELLOW)

Time period [T]	Time [s]	Voltage [V]	C2 [V]
T = 0	0.00	5.72	5.372
$\frac{1}{2} T$	0.900	-7.04	-1.264
T	1.8	5.72	5.372

TABLE 2 - MEASURED VALUES FROM BREAD BOARD CIRCUIT

The values in

Table 2 were calculated by multiplying the change in y values in one cycle by 'volts per division' and the change in x values in one cycle by 'seconds per division' [6]. The maximum voltage at $T = 0$ is therefore calculated as $2.2Vdiv^{-1} \times 2.6div = 5.72V$; and $1/2T$ can be calculated as $200mSdiv^{-1} \times 4.5div = 900mS$.

DISCUSSION

Table 3 allows for comparison between the simulated and bread board circuits. There is a discrepancy between the data which could be due to manufacturing tolerances affecting the accuracy of the selected components. The components used in proteus may also differ slightly to the ones used in the breadboard despite nominally being the same specification. Ambient temperature and changes of temperature within the components themselves may also contribute a degree of error to the breadboard circuit.

Time period [T]	Time [s]		Voltage [V]		C1 [V]	
	Simulation	Breadboard	Simulation	Breadboard	Simulation	Breadboard
T = 0	0.00	0.00	5.45	5.72	1.35	5.372
½ T	0.760	0.900	-5.75	-7.04	-1.5	-1.264
T	1.46	1.8	5.45	5.72	1.35	5.372

TABLE 3 - COMPARISON OF VALUES

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