



2

12 Pages

1. Please give the information requested in the boxes below.
2. Enter your name in the space provided to the right, fold over and seal down (using the label provided) to hide your name.
3. The answers must be legibly written. The Examiners can either ignore the script or have it typed and the expense of typing charged to the candidate.
4. Write your answers in ink.
5. Begin each answer on a fresh page. Do all rough work in the answer book and cross it through.
6. No part of this book is to be torn out; it must be handed in complete.
7. If more books than one are used, fasten them together using the tags available from the invigilator(s).
8. **Every book must be handed in. In no circumstances may answer books, used or unused, be taken out of the examination venue.**

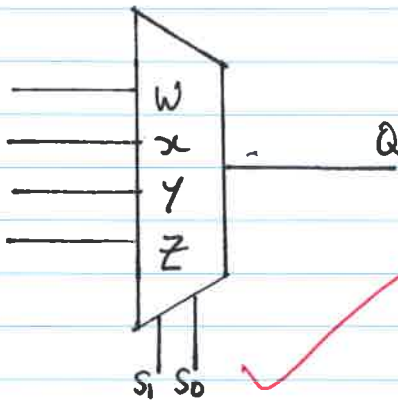
[illegible]

(Gweler yr ochr arall am y fersiwn Cymraeg)

$\frac{73}{100}$

Q1 i)

a)



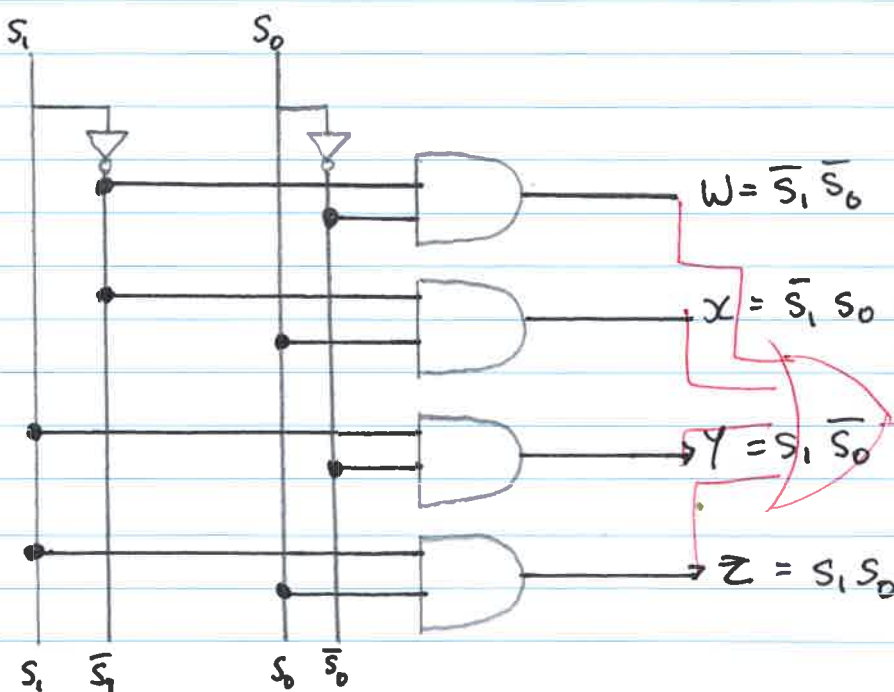
b)

S_1	W	X	Y	Z	S_1	S_0
0	0	0	1		0	0
0	0	1	0		0	1
0	1	0	0		1	0
1	0	0	0		1	1

Z	Y	X	W	S_1	S_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

$$\begin{aligned} W &= \bar{S}_1 \bar{S}_0 \\ X &= \bar{S}_1 S_0 \\ Y &= S_1 \bar{S}_0 \\ Z &= S_1 S_0 \end{aligned}$$

c)



Q1
ii)

IEEE Std. logic. 1164, ALL

Entity mux - is

Port (A, B, C, D in: Bit;
S₁, S₀ in: Bit;
Q out: Bit);

end mux.

architecture of Dataflow of mux is

begin;

Process (A, B, C, D, S₁, S₀, Q)
begin;

if (S₁ = '0' and S₀ = '0') then

Q <= 'A';

else if (S₁ = '0' and S₀ = '1') then

Q <= 'B';

else if (S₁ = '1' and S₀ = '0') then

Q <= 'C';

else;

Q <= 'D';

end process;

end Dataflow;

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20

10

Phit y Cwestiwn

P. 14

Q2
i)

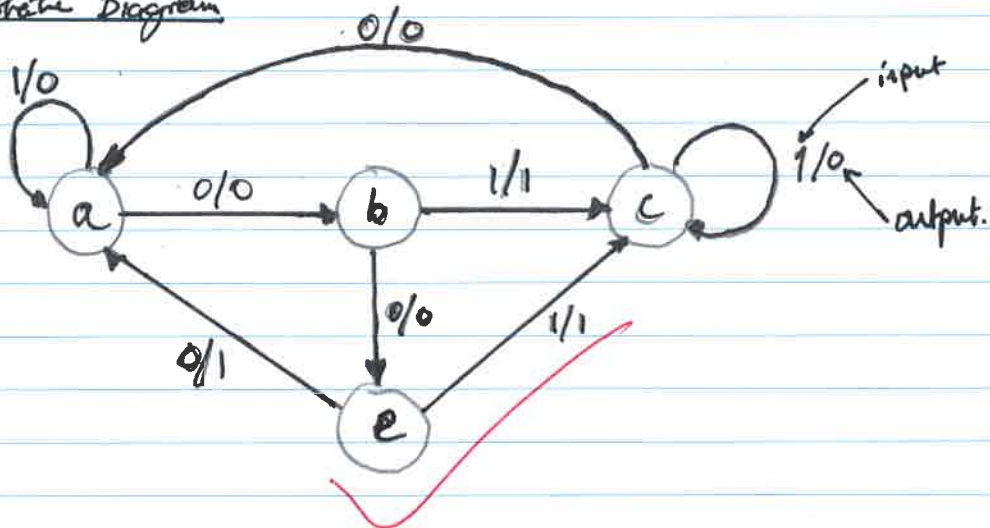
Present state (PS)	Next State (NS)		Output (Q)	
	X=0	X=1	X=0	X=1
a	b	d	0	0
b	e	c	0	1
c	d	c	0	0
d	b	d	0	0
e	a	c	1	1

States a and d Repeating. Replace all d by a.

Present state (PS)	Next state (NS)		Output (Q)	
	X=0	X=1	X=0	X=1
a	b	a	0	0
b	e	c	0	1
c	a	c	0	0
e	a	c	1	1

No more Repeating states.

Reduced State Diagram



Q2

ii)

a) State assignment:

$$a = 00$$

$$b = 01$$

$$c = 10$$

$$d = 11$$

b) State table

	Present state	x	Next state	Output (a)
a	0 0	0	0 1	0
	0 0	1	0 0	0
b	0 1	0	1 1	0
	0 1	1	1 0	1
c	1 0	0	0 0	0
	1 0	1	1 0	0
d	1 1	0	0 0	1
	1 1	1	1 0	1

c) Excitation table using D flip Flop.

Present state		x	Next state	Q	D ₁	D ₂
A	B					
0	0	0	0 1	0	0	1
0	0	1	0 0	0	0	0
0	1	0	1 1	0	1	1
0	1	1	1 0	1	1	0
1	0	0	0 0	0	0	0
1	0	1	1 0	0	1	0
1	1	0	0 0	1	0	0
1	1	1	1 0	1	1	0

Q2

Q2

output expression.D₁

A	B	x	0	1
0	0		0	0
0	1		1	1
1	1		0	1
1	0		0	1

$$D_1 = \bar{A}B + Ax$$

D₂

A	B	x	0	1
0	0		1	0
0	1		1	0
1	1		0	0
1	0		0	0

$$D_2 = \bar{A}\bar{x}$$

Q

A	B	x	0	1
0	0		0	0
0	1		0	1
1	1		1	1
1	0		0	0

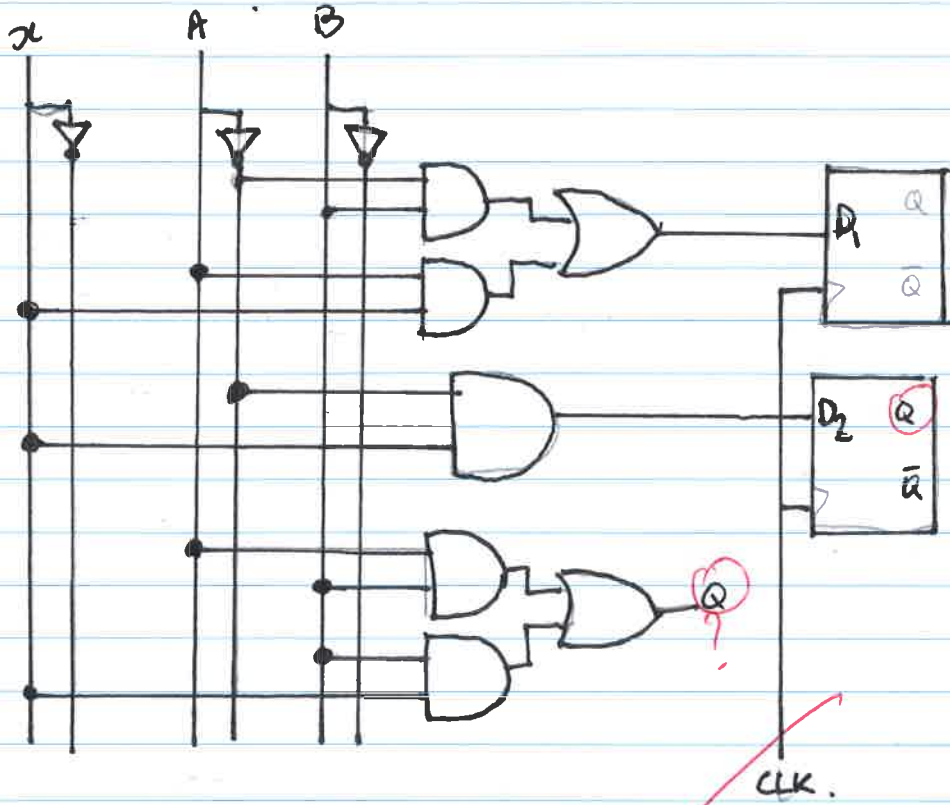
$$Q = AB + Bx$$

3

3

Q2

e)



3

19/20

3

Q2 = 19

Q3

i) $-5 \neq 5 = 0101$
 1's complement = 1010
 2's complement = 1011
 $\therefore -5 = 1011$

ii)

IEEE Std Logic 1164. All.

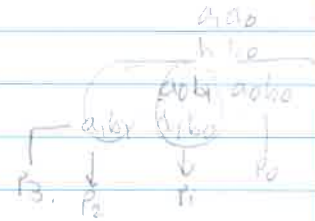
entity multiplier is

Port (A, B in: Bit_Vector (1 down to 0));
 P out: Bit_Vector (3 down to 0);

end multiplier;

architecture of multiplier is behavioural of multiplier is
begin $P(0) \leftarrow (A[0] \text{ and } B[0]);$ $P(1) \leftarrow (A_0 \text{ and } B_1) \text{ xor } (A_1 \text{ and } B_0);$ $P(2) \leftarrow (A_1 \text{ and } B_1) \text{ xor } ((A_0 \text{ and } B_1) \text{ and } (A_1 \text{ and } B_0));$ $P(3) \leftarrow (A_1 \text{ and } B_1) \text{ and } ((A_0 \text{ and } B_1) \text{ and } (A_1 \text{ and } B_0));$

end behavior



half adder

Sum = A xor B

carry = A and B

2

4

08
20

8

Rhif y Cwestiwn

08
20

Q5

i)

a)

x	y	z	F_1
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

x	y	z	F_2
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

b)

 F_1

x \ y \ z	0	1
0	0	1
0	1	0
1	1	0
1	0	1

$$F_1 = \bar{x}\bar{y}\bar{z} + \bar{x}yz + x\bar{y}\bar{z} + x\bar{y}z$$

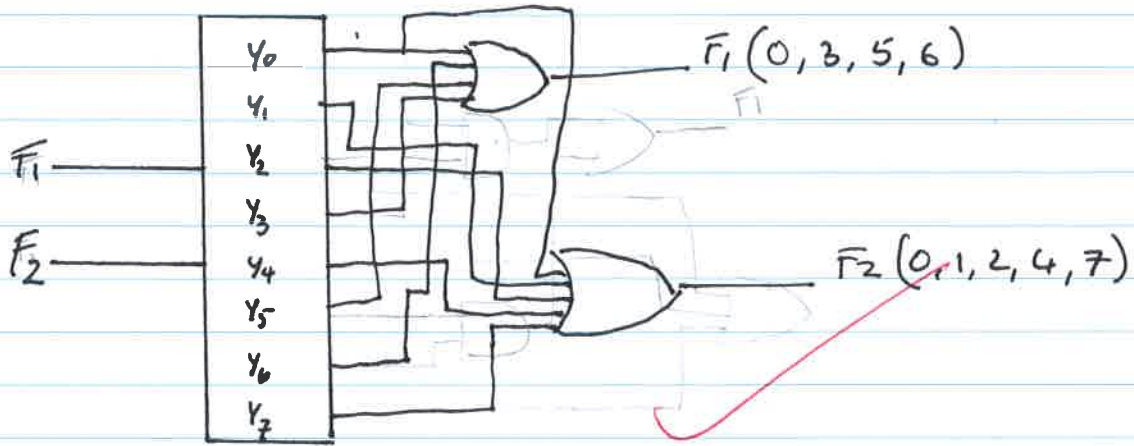
 F_2

x \ y \ z	0	1
0	1	1
0	1	0
1	0	1
1	1	0

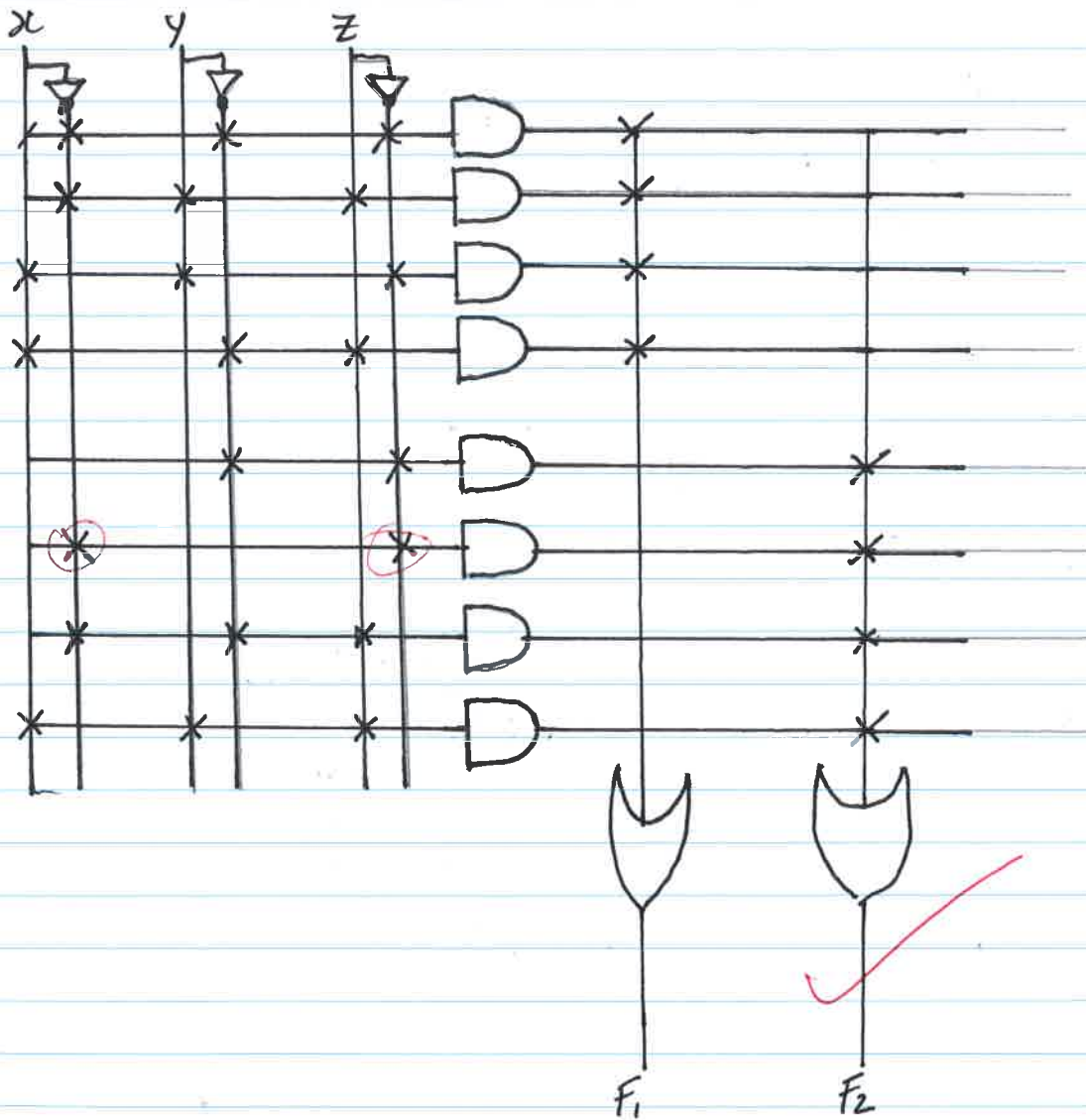
$$F_2 = \bar{y}\bar{z} + \bar{x}\bar{z} + \bar{x}\bar{y}z + x\bar{y}z$$

Q5

c)



d) Design using PLA.

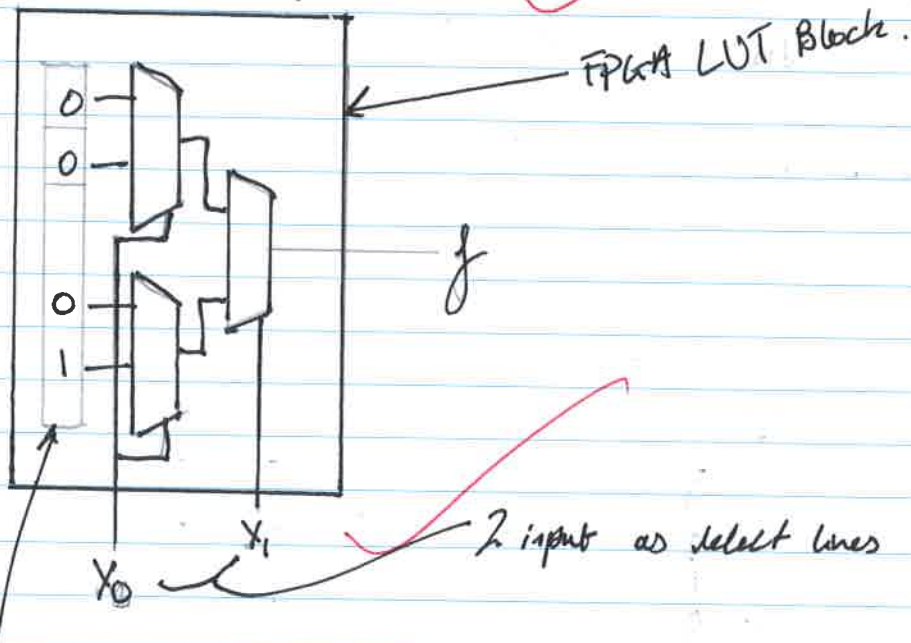


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Q6
i)

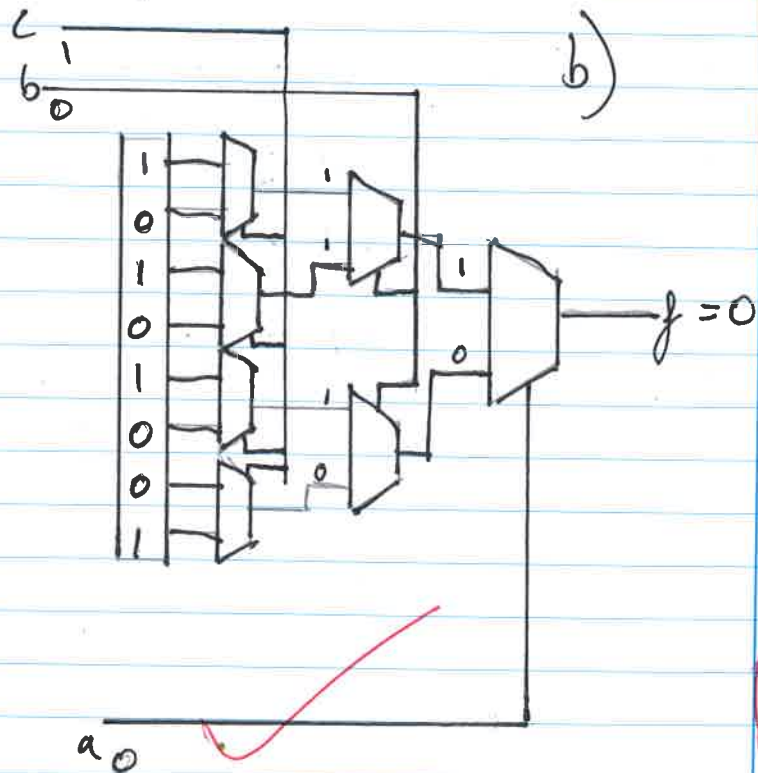
LUT or look up tables are the logic blocks of an FPGA. They contain a storage block with each cell connected to the input of a two input multiplexer. They can perform any logic task by the use of the select lines.



Storage block for truth table output

ii)
a)

A	B	C	f
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1



$f = 0$ for $abc = 001$