



Prifysgol Cymru
Y Drindod Dewi Sant
University of Wales
Trinity Saint David

Examination Answer Books

12 Pages

Instructions to Candidates

1. Please give the information requested in the boxes below.
2. Enter your name in the space provided to the right, fold over and seal down (using the label provided) to hide your name.
3. The answers must be legibly written. The Examiners can either ignore illegible script or have it typed and the expense of typing charged to the candidate.
4. Write your answers in ink.
5. Begin each answer on a fresh page. Do all rough work in the answer book and cross it through.
6. No part of this book is to be torn out; it must be handed in complete.
7. If more books than one are used, fasten them together using the tags available from the invigilator(s).
8. Every book must be handed in. In no circumstances may answer books, used or unused, be taken out of the examination venue.

Complete, fold and seal
(see note 2 below)

SURNAME: Mills

FORENAME(S): William

1	Student Number	2219605
2	Title of Examination Paper	Micros peripherals and Interfaces
3	Module Code	ACDA4004
4	Date and Time of Examination	12/05/2023 09:00 AM
5	Examination Venue	310
6	Seat Number	005
7	Number of Answer Books handed in	

List the numbers of the questions you have attempted	Office Use
1	
4	
5	
17	
3	
Total	15

$\times 2 = 30\%$

(Gweler yr ochr arall am y fersiwn Cymraeg)

Q1.

a) BSF - Backup Store Function

x

x

b) ~~BSF~~ BTFSC -

x

x

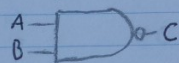
c) ANDLW - And ~~to~~ List Word

d) MOVWF - Move Word Function

e) INCF -

Q.4

Logic Symbol for a NAND



Truth table

A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

Examiner Only

Question No.

Q.5

Truth Tables

(In the case of this circuit, I will be referring to the top logic gate output as D. Similarly, I will refer to the bottom logic gate output as E)

A	B	D	A	B	E
0	0	0	0	0	0
0	1	0	0	1	0
1	0	0	1	0	1
1	1	1	1	1	0

D	E	Q
0	0	0
0	0	0
0	1	1
1	0	1

Examiner Only

8

Q.7 The uses for the 'data', 'address' and 'control' busses in a Von Neumann architecture are fairly straight forward. The 'data' bus will be where all data comes from and goes to, almost like ~~an~~ a random memory access unit. However, the 'address' bus will be a receiver of the data, being used ~~to~~ ~~to~~ ~~to~~ to address and separate data, essentially processing it as needed. Finally, the 'control' bus is what controls the flow of data in and out of the ~~bus~~ architecture, whether it be ~~entering~~ ~~the~~ data entering or exiting the system.

Too Vague!

Q.3 An ADC ~~converter~~ is in simpler terms an Analogue to Digital Converter. What this means ~~is~~ is that it will take an analogue input and process it into a digital format, which will then be output into whatever system the ADC ~~is~~ is a part of. This is done by ^{counting} basically counting, the way the circuit ~~counts~~ is with the use of its 'clock input', which is a piece that ticks a certain amount of times indefinitely, until the system turns off. The output results of this clock is input into a 'binary counter', allowing the data collected from the clock to be coherent, as the binary value ~~increases~~ increases with each tick of the 'clock input'.

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