

## LEVEL 4 ASSESSMENT SPECIFICATION

|                                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |                                                      |                |
|---------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------|----------------|
| Student name:                   | Chloe Price                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | Student ID number:                                   |                |
| Programme:                      | HNC Electrical/Electronic Engineering                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                                                      |                |
| Module:                         | Electronics                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |                                                      |                |
| Module code:                    | PCEE4006                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | Contribution to Overall Module Assessment (%):       | 50%            |
| Lecturer:                       | Jason Pointer                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | Internal Verifier:                                   | Nigel Richards |
| Assignment Title:               | Digital Systems                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Word count (or equivalent):                          | 2000           |
| Submission deadline:            | 11/05/23                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | Return date of provisional marks & written feedback: | 25/05/23       |
| Submission method:              | <p>All written assessments, where practical and possible, must be submitted via Turnitin unless otherwise instructed by the Lecturer. (Please DO NOT put this assessment specification into Turnitin or it will match many similarities with other students' submissions.)</p> <p><b>Alternative submission method (if applicable):</b></p> <p><b>Late submission of the assessment will result in a late penalty mark.</b> Penalties for late submission: Up to one week late, maximum mark of 40%. Over one week late, 0%. Only the Extenuating Circumstances Panel may approve a change to submission dates.</p> |                                                      |                |
| Academic honesty / referencing: | <p>Academic honesty is required. In the main body of your submission you must give credit to authors on whose research and ideas your work is based. Append to your submission a reference list that indicates the books, articles, etc. that you have used, cited or quoted in order to complete this assessment.</p>                                                                                                                                                                                                                                                                                              |                                                      |                |

### Module Learning Outcomes (from module syllabus)

1. Demonstrate an understanding of semi-conductor components and characteristics and their application in analogue and **digital** electronic circuits.
2. To design, simulate, build, test and evaluate analogue and **digital** electronic circuits using information gained from datasheets.

# STUDENT FEEDBACK FORM

This section details the *extent* to which the assessment criteria are demonstrated by you, which in turn determines your mark. The marks available for each category of skill are shown. Lecturers will use the space provided to comment on the achievement of the task(s), including those areas in which you have performed well and areas that would benefit from development/improvement.

| Generic Assessment Criteria                                                                                                                                                                                                                                                                               | Marks available | Marks awarded |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|---------------|
| <b>1. Engagement with Literature Skills</b>                                                                                                                                                                                                                                                               | 10              | 0.5           |
| Little or no evidence of reading only listed a couple of websites and no direct referencing within the assignment.                                                                                                                                                                                        |                 |               |
| <b>2. Knowledge and Understanding Skills</b>                                                                                                                                                                                                                                                              | 45              | 28.6          |
| Task 1 & 2 achieved 60%.<br>Task 3 & 4 achieved 67%.<br>Knowledge of the basic underlying concepts and principles is competent with a very good understanding in most aspects of digital systems. Showed very good understanding the logic gates, Boolean algebra, Karnaugh maps and counter design work. |                 |               |
| <b>3. Cognitive and Intellectual Skills</b>                                                                                                                                                                                                                                                               | 10              | 4             |
| Some evidence to support emerging arguments and judgements but in some places they are underdeveloped or missing.                                                                                                                                                                                         |                 |               |
| <b>4. Practical Application Skills</b>                                                                                                                                                                                                                                                                    | 25              | 18.3          |
| Task 1 & 2 achieved 66%.<br>Task 3 & 4 achieved 80%.<br>A very good application of practical work for most tasks, very good use of the test equipment and Multisim to obtain the required test results. In Task 1 have not included all of the Multisim results                                           |                 |               |
| <b>5. Transferable Skills for Life and Professional Practice</b>                                                                                                                                                                                                                                          | 10              | 6             |
| Work is accurate, coherent, fluent, well-structured and organised.                                                                                                                                                                                                                                        |                 |               |

|                                                                                                                                                                                                            |                                                        |  |            |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------|--|------------|
| <b>Assessment Mark</b> (Assessment marks are subject to ratification at the Exam Board. These comments and marks are to give feedback on module work and are for guidance only until they are confirmed. ) | <b>Late Submission Penalties (tick if appropriate)</b> |  | <b>57%</b> |
|                                                                                                                                                                                                            | Up to 1 week late (40% Max)                            |  |            |
|                                                                                                                                                                                                            | Over 1 week late (0%)                                  |  |            |



# Digital Systems

HNC ELECTRICAL AND ELECTRONIC ENGINEERING -  
ELECTRONICS  
CHLOE PRICE

JASON POINTER

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| Bibliography .....                                          | 18                                  |

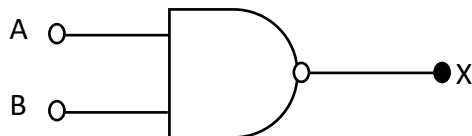
## Introduction

Digital systems play a fundamental role in modern technological landscape. This assignment serves as an introduction to digital systems, providing a comprehensive overview of their basic concepts, components, and applications. We will explore the fundamental principles of digital logic, the building blocks of digital systems, and how they enable the processing and manipulation of binary information. Additionally, we will delve into various types of digital systems, such as combinational and sequential circuits, as well as their practical implementation using integrated circuits. ✓

## Task 1 – Combination Logic

Using Multisim construct and test the following circuits. For each circuit complete a truth table and measure the logic value at each point indicated in the truth table. Write down the simplified Boolean expression and check that the measured values agree with the expected values.

(a)

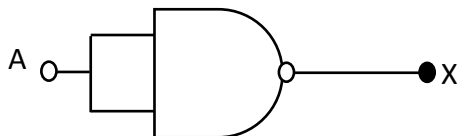


| A | B | X |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

$$X = \bar{A}.\bar{B} + \bar{A}.B + A.\bar{B}$$

$$X = \overline{A.B}$$

(b)

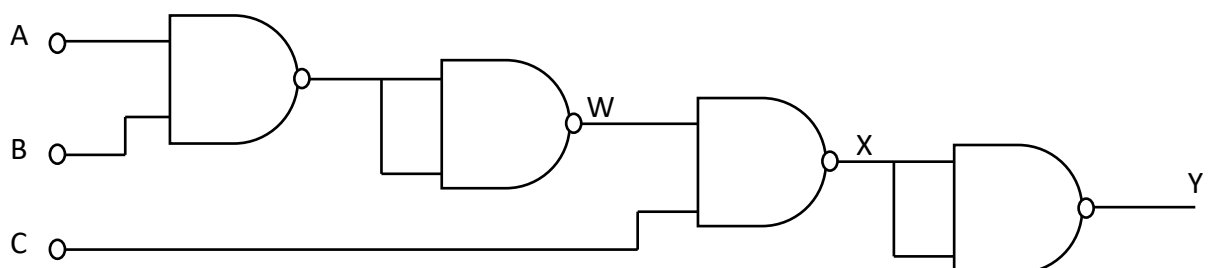


| A | X |
|---|---|
| 0 | 1 |
| 1 | 0 |

$$X = \bar{A}$$

*Have not shown the Multisim results*

(c)



| A | B | C | W | X | Y |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 | 0 | 1 |

$$W = A.B$$

This is a 2 input AND gate.

$$X = \overline{A.B.C}$$

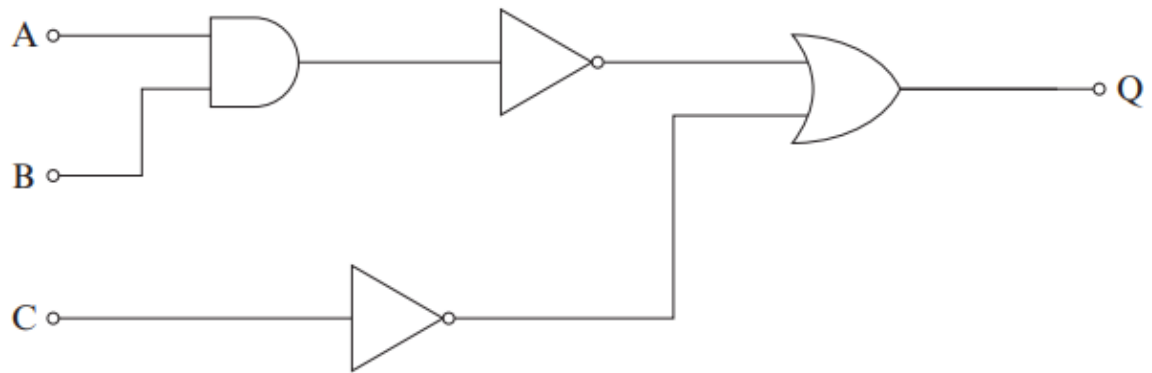
This is a 3 input NAND gate.

$$Y = A.B.C$$

This is a 3 input AND gate.

State the logic function for W, X and Y and simplify.

(d) Produce the truth table and Boolean expression for the circuit shown below.



| A | B | C | Q |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

$$Q = \overline{A.B.C}$$

Draw the NAND gate equivalent circuit for the circuit shown above using only 2-input NAND gates, show how it can be simplified and use Multisim to confirm its results.

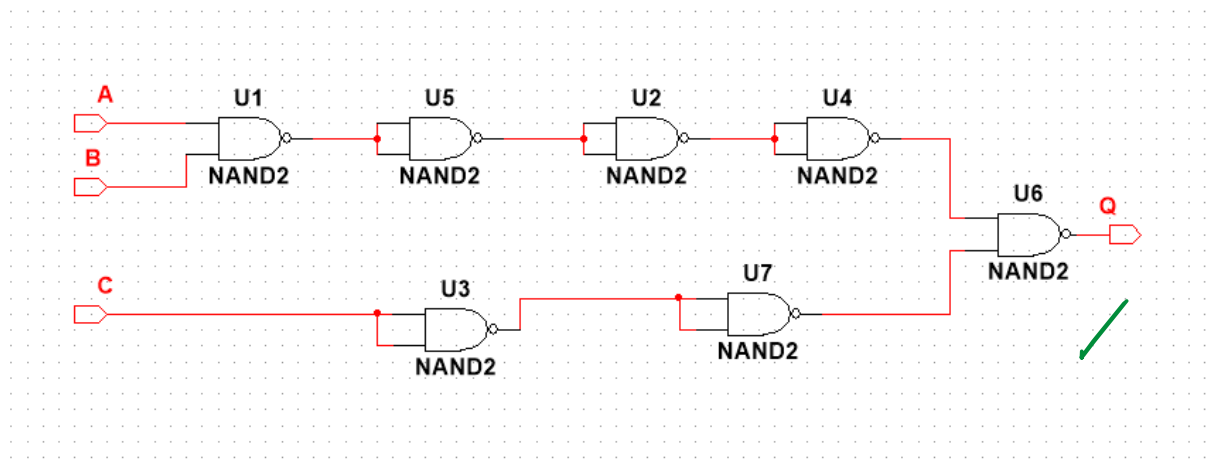


Figure 1

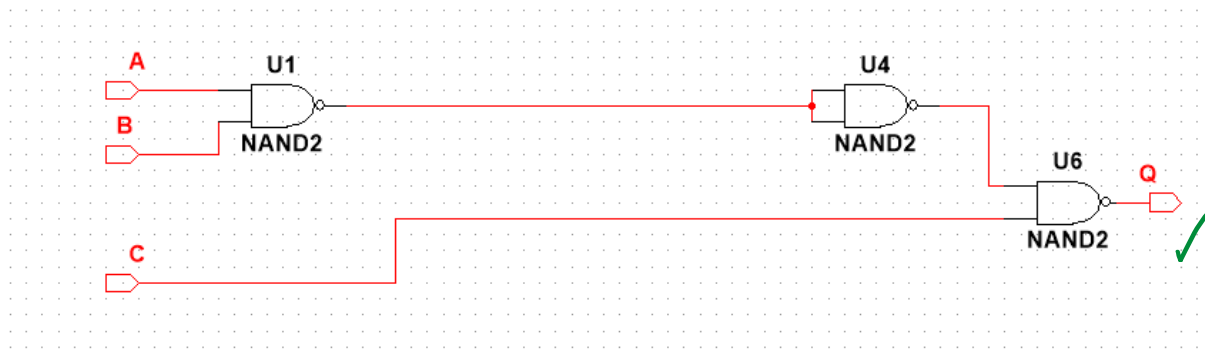


Figure 2

Well done.

Explain the benefit of using the NAND gate equivalent circuit:

The NAND gate is a fundamental building block of digital electronics and is used to implement many other digital circuits. The NAND gate equivalent circuit is a way of representing a digital circuit using only NAND gates, which provides several benefits. ✓

Reduced component count: Using only NAND gates in a circuit can significantly reduce the number of components required to implement the circuit. This is because many other digital logic gates can be implemented using NAND gates alone. ✓

Ease of modification: using the NAND gate equivalent circuit makes it easier to modify or upgrade the circuit in the future. Since the circuit is composed entirely of NAND gates, changes can be made by simply replacing one or more NAND gates with different ones. This is simpler than having to modify multiple types of gates. ✓

- (e) Simplify the following Boolean equations, ONLY using the LAWS OF BOOLEAN ALGEBRA and DeMORGANS THEOREM. Verify your findings by using Multisim constructing the logic circuits using NAND gates.

i)  $Q = (A+B) (A + \bar{B}) (\bar{A} + C)$

$$Q = (A + A.\bar{B} + B.A + B.\bar{B}).(\bar{A} + C)$$

$$= (A + A.\bar{B} + A.B).(\bar{A} + C)$$

$$= (A.(1 + \bar{B} + B)).(\bar{A} + C)$$

$$= A.1.(\bar{A} + C)$$

$$= A.(\bar{A} + C)$$

$$= A.\bar{A} + A.C$$

$$Q = A.C$$

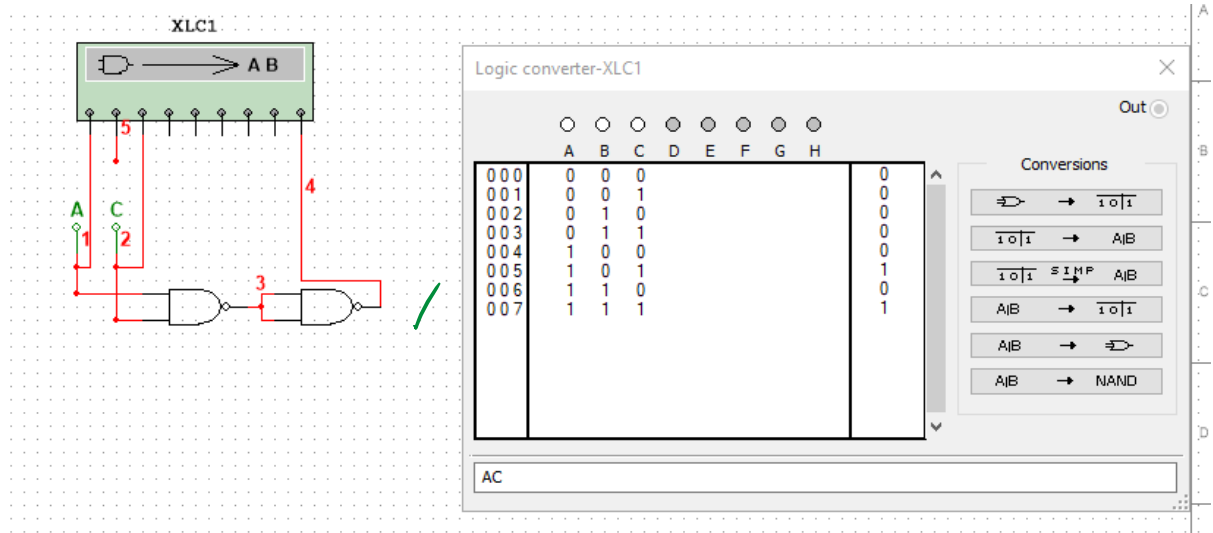


Figure 3

$$\begin{aligned}
 \text{ii) } Q &= A.B.\bar{C} + A.\bar{C} + \bar{A}.\bar{C}.D + \bar{A}.\bar{C}.\bar{D} \\
 &= \bar{C}.(A.B + A + \bar{A}.D + \bar{A} + \bar{D}) \\
 &= \bar{C}.(A(B + 1) + \bar{A}.(D + \bar{D})) \\
 &= \bar{C}.(A + \bar{A}) \\
 &= \bar{C}
 \end{aligned}$$

The screenshot shows the Logic Converter-XLC1 interface. It features a truth table with 16 rows (000 to 111) and 8 columns (A, B, C, D, E, F, G, H). The output column (Q) is labeled 'Out' and has a value of 1 for all input combinations. The logic expression entered in the bottom field is  $A'CD' + AC' + C'D$ . The 'Conversions' panel on the right shows various logic symbols and their corresponding expressions, including  $\overline{A|B}$  and  $A|B$ .

|     | A | B | C | D | E | F | G | H | Out |
|-----|---|---|---|---|---|---|---|---|-----|
| 000 | 0 | 0 | 0 | 0 |   |   |   |   | 0   |
| 001 | 0 | 0 | 0 | 1 |   |   |   |   | 1   |
| 002 | 0 | 0 | 1 | 0 |   |   |   |   | 1   |
| 003 | 0 | 0 | 1 | 1 |   |   |   |   | 0   |
| 004 | 0 | 1 | 0 | 0 |   |   |   |   | 0   |
| 005 | 0 | 1 | 0 | 1 |   |   |   |   | 1   |
| 006 | 0 | 1 | 1 | 0 |   |   |   |   | 1   |
| 007 | 0 | 1 | 1 | 1 |   |   |   |   | 0   |
| 008 | 1 | 0 | 0 | 0 |   |   |   |   | 1   |
| 009 | 1 | 0 | 0 | 1 |   |   |   |   | 1   |
| 010 | 1 | 0 | 1 | 0 |   |   |   |   | 0   |
| 011 | 1 | 0 | 1 | 1 |   |   |   |   | 0   |
| 012 | 1 | 1 | 0 | 0 |   |   |   |   | 1   |
| 013 | 1 | 1 | 0 | 1 |   |   |   |   | 1   |

Logic expression:  $A'CD' + AC' + C'D$

Figure 4

*This table is incorrect for  $\bar{C}$ .*

- (f) Binary Coded Decimal (BCD) is a 4-bit binary code with the range of numbers 1010 to 1111 not used. Design a circuit that will detect these invalid codes. Construct the circuit and verify that it performs the required task.

| A | B | C | D | Q |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 |

|   |   |   |   |   |
|---|---|---|---|---|
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |



$$Q = A.\bar{B}.C.\bar{D} + A.\bar{B}.C.D + A.B.\bar{C}.\bar{D} + A.B.\bar{C}.D + A.B.C.\bar{D} + A.B.C.D$$



Karnaugh map:

| AB \ CD | 00 | 01 | 11 | 10 |
|---------|----|----|----|----|
| 00      |    |    |    |    |
| 01      |    |    |    |    |
| 11      | 1  | 1  | 1  | 1  |
| 10      |    |    | 1  | 1  |



**Simplified Boolean Algebra:**

$$Q = A.B + A.C$$



## DeMorgans Theorem:

Invert all

$$\bar{Q} = \overline{A \cdot B + A \cdot C}$$

$$\bar{Q} = \overline{A \cdot B} \cdot \overline{A \cdot C}$$

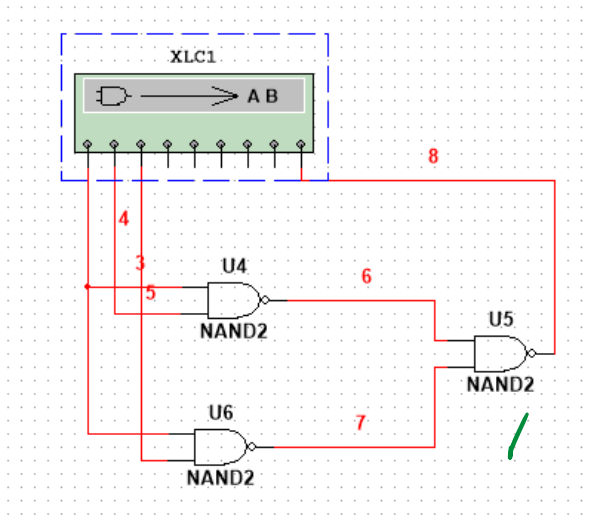


Figure 6

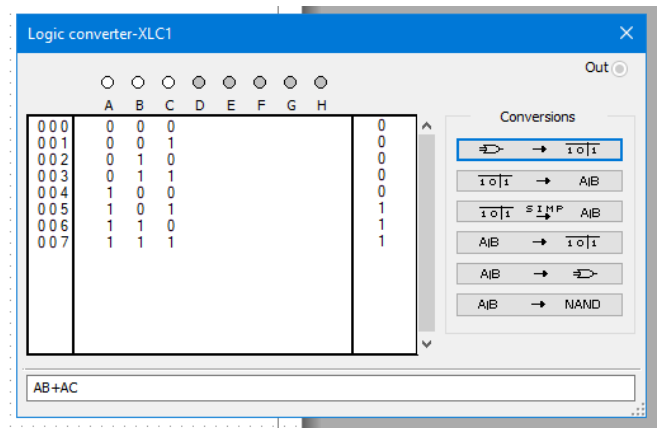


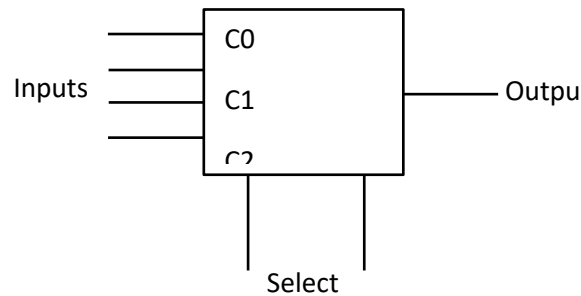
Figure 5

Invert Again

$$Q = \overline{\overline{A \cdot B} \cdot \overline{A \cdot C}}$$

## Task 2 – Multiplexer

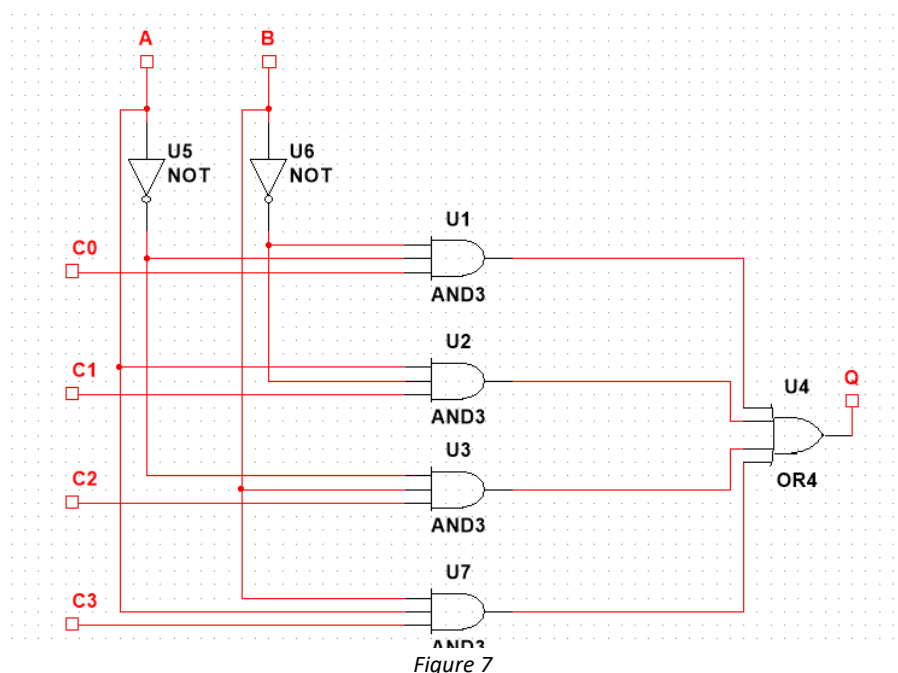
An arrangement where several inputs can be connected but only one input, under the influence of a select input, will have access to the output. The block diagram below shows a 4-to-1 multiplexer, produce a truth table and the Boolean equation to representation the multiplexer. Use this information to design the 4-to-1 multiplexer using logic gates and test its function using Multisim.



Multiplexer Truth Table:

| Input | Switch Selector |   | Output Q |
|-------|-----------------|---|----------|
|       | A               | B |          |
| $C_0$ | 0               | 0 | $C_0$    |
| $C_1$ | 0               | 1 | $C_1$    |
| $C_2$ | 1               | 0 | $C_2$    |
| $C_3$ | 1               | 1 | $C_3$    |

$$Q = C_0 \cdot \bar{A} \cdot \bar{B} + C_1 \cdot \bar{A} \cdot B + C_2 \cdot A \cdot \bar{B} + C_3 \cdot A \cdot B$$



*You need a commit about testing*

## Task 3 – Sequential Logic

### The truth table of the D-type and J-K Flip-Flop

- Construct the following debouncing circuit, and connect the clock of a D-type flip-flop to the output. Monitoring the clock, Q and  $Q_{\text{BAR}}$  outputs with LEDs and complete Table 1.
- Now connect the clock of J-K flip-flop to the output. Monitoring the clock, Q and  $Q_{\text{BAR}}$  outputs with LEDs and complete Table 2.

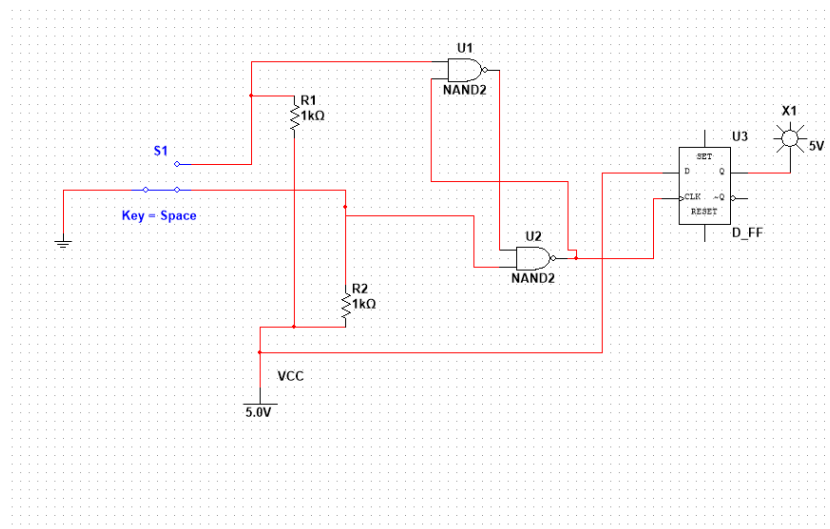
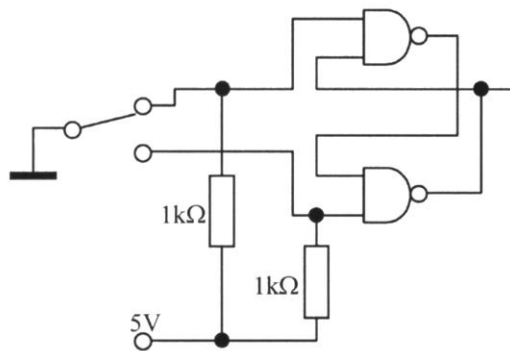


Figure 8

Table 1 - D-type truth table

| Input | Outputs |           |
|-------|---------|-----------|
| D     | Q       | $\bar{Q}$ |
| 0     | 0       | 1         |
| 1     | 1       | 0         |

Table 2 – J-K truth table

| Input |   | Outputs   |           |
|-------|---|-----------|-----------|
| J     | K | Q         | $\bar{Q}$ |
| 0     | 0 | no change | No change |
| 0     | 1 | 0         | 1         |
| 1     | 0 | 1         | 0         |
| 1     | 1 | toggle    | toggle    |

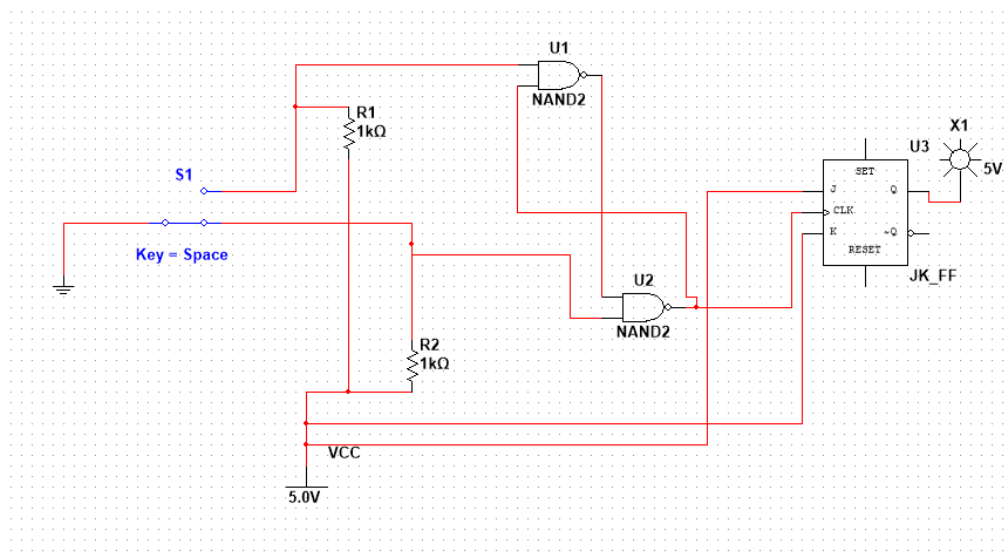


Figure 9

- (c) The cross-coupled NAND gates are for switch debouncing. Why are they needed and how do they work?

Cross-coupled NAND gates, are commonly used in digital circuits for switch debouncing. Switch debouncing is a technique used to eliminate or reduce the effect of mechanical switch bounce, which occurs when a switch is rapidly opened or closed.

When a mechanical switch is pressed or released, the contacts can bounce multiple times before settling into a stable state. This bouncing can create multiple open-close transitions in a short period, leading to erroneous or unstable readings in digital circuits. Switch debouncing helps eliminate these unwanted transitions and ensures a clean and reliable signal.

Cross coupled NAND gates provide a simple and effective way to debounce a switch. The basic principle behind their operation is positive feedback.

By utilizing the positive feedback loop and the inherent delay in the gates' operation, cross-coupled NAND gates provide a stable output state and filter out the rapid transitions caused by switch bounce. The debounced signal can then be used reliably in digital circuits without the risk of false triggers or unstable readings.



## Task 4 – Using Sequential Logic to solve Real problems

Design and simulate a 3-stage synchronous binary counter using JK flip-flops that will produce the even numbers (including zero) in the range 0 to 7.

Designing a counter

Excitation table

| Present Q | Next Q | J | K |
|-----------|--------|---|---|
| 0         | 0      | 0 | X |
| 0         | 1      | 1 | X |
| 1         | 0      | X | 1 |
| 1         | 1      | X | 0 |

Design a counter that goes from 0 to 6 even numbers.

|   | Present |       |       | Next  |       |       |       |       |       |       |       |       |
|---|---------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
|   | $Q_A$   | $Q_B$ | $Q_C$ | $Q_A$ | $Q_B$ | $Q_C$ | $J_A$ | $K_A$ | $J_B$ | $K_B$ | $J_C$ | $K_C$ |
| 0 | 0       | 0     | 0     | 0     | 1     | 0     | 0     | X     | 1     | X     | 0     | X     |
| 2 | 0       | 1     | 0     | 1     | 0     | 0     | 1     | X     | X     | 1     | 0     | X     |
| 4 | 1       | 0     | 0     | 1     | 1     | 0     | X     | 0     | 1     | X     | 0     | X     |
| 6 | 1       | 1     | 0     | 0     | 0     | 0     | X     | 1     | X     | 1     | 0     | X     |

The excitation truth table demonstrates the design of the JK flip flops that are needed to be connected together to each other and external power inputs.

From the excitation truth tables Karnaugh maps have been produced for  $J_A$ ,  $K_A$ ,  $J_B$ ,  $K_B$ ,  $J_C$ , and  $K_C$ .

Karnaugh Map for  $J_A$ :

| $Q_A \backslash Q_B Q_C$ | 00 | 01 | 11 | 10 |
|--------------------------|----|----|----|----|
| 0                        | 0  | x  | x  | 1  |
| 1                        | x  | x  | x  | x  |

$$J_A = B$$

Karnaugh Map for  $K_A$ :

| $Q_A \backslash Q_B Q_C$ | 00 | 01 | 11 | 10 |
|--------------------------|----|----|----|----|
| 0                        | x  | x  | x  | x  |
| 1                        | 0  | x  | x  | 1  |

$$K_A = B$$

Karnaugh Map for  $J_B$ :

| $Q_A \backslash Q_B Q_C$ | 00 | 01 | 11 | 10 |
|--------------------------|----|----|----|----|
| 0                        | 1  | x  | x  | x  |
| 1                        | 1  | x  | x  | x  |

$$J_B = 1$$

Karnaugh Map for  $K_B$ :

| $Q_A \backslash Q_B Q_C$ | 00 | 01 | 11 | 10 |
|--------------------------|----|----|----|----|
| 0                        | x  | x  | x  | 1  |
| 1                        | x  | x  | x  | 1  |

$$K_B = 1$$

Karnaugh Map for  $J_C$ :

| $Q_A \backslash Q_B Q_C$ | 00 | 01 | 11 | 10 |
|--------------------------|----|----|----|----|
| 0                        | 0  | x  | x  | 0  |
| 1                        | 0  | x  | x  | 0  |

$$J_C = 0$$

Karnaugh Map for  $K_C$ :

| $Q_A \backslash Q_B Q_C$ | 00 | 01 | 11 | 10 |
|--------------------------|----|----|----|----|
| 0                        | x  | x  | x  | x  |
| 1                        | x  | x  | x  | x  |

$$K_C = 0$$

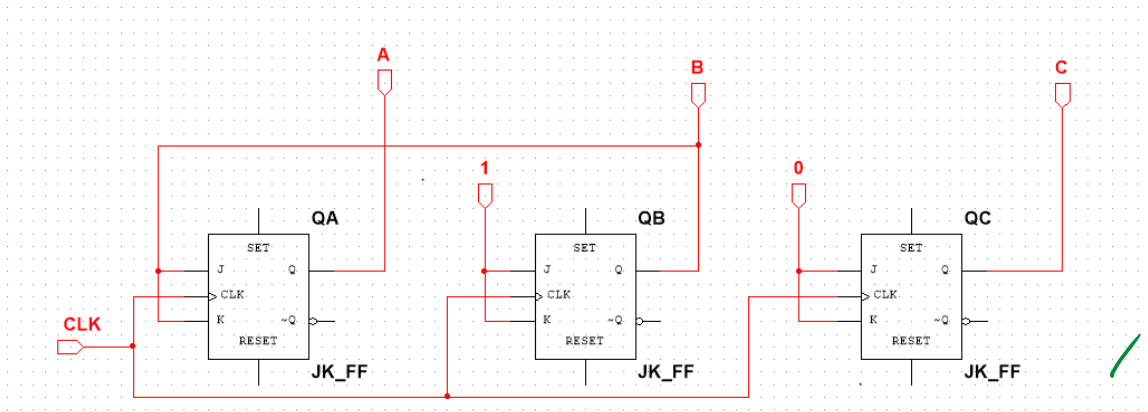


Figure 10

Below the count sequence generated from the circuit.

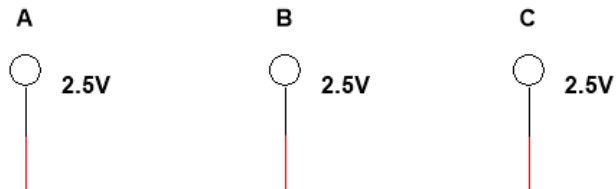


Figure 11 - 0

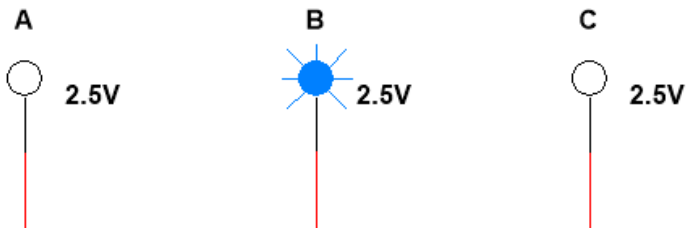


Figure 12 - 2

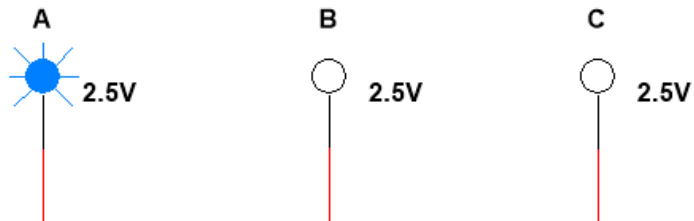


Figure 13 - 4

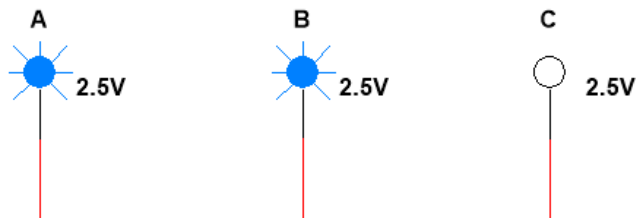


Figure 14 - 6

The above figures show the JK flip flops working correctly and producing the results in the Karnaugh maps above, we were able to make a simple circuit to produce the results.

## Bibliography

Electronic Circuits and Diagrams-Electronic Projects and Design. n.d. *What are Digital Logic Gates and their types?*. [online] Available at: <<https://www.circuitstoday.com/logic-gates>>.

All About Circuit. *The J-K Flip-Flop*. [online] Available at:

<<https://www.allaboutcircuits.com/textbook/digital/chpt-10/j-k-flip-flop/>>

*You have not stated any references.*