



Complete, fold and seal
(see note 2 below)

FORENAME(S): RYAN

Instructions to Candidates

1. Please give the information requested in the boxes below.
2. Enter your name in the space provided to the right, fold over and seal down (using the label provided) to hide your name.
3. The answers must be legibly written. The Examiners can either ignore illegible script or have it typed and the expense of typing charged to the candidate.
4. Write your answers in ink.
5. Begin each answer on a fresh page. Do all rough work in the answer book and cross it through.
6. No part of this book is to be torn out; it must be handed in complete.
7. If more books than one are used, fasten them together using the tags available from the invigilator(s).
8. **Every book must be handed in. In no circumstances may answer books, used or unused, be taken out of the examination venue.**

[illegible]

(Gweler yr ochr arall am y fersiwn Cymraeg)

State Model

Q2

	00	01	11	10
0	0	$\bar{D}$	1	1
1	0	0	0	1

$$F = \bar{B}\bar{C}\bar{D} + ABD + A\bar{B}$$

$$F = \bar{A}\bar{C}\bar{D} + ABD + A\bar{B}$$

$$SOP = B\bar{C}\bar{D} + ABD + A\bar{B}$$

$$F_{full} = \bar{A}\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C} + A\bar{B}C + ABCD + A\bar{B}C$$

4 ✓

A	B	C	D
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1

A	B	C	D
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

Full Short Sop

$\bar{A}\bar{B}\bar{C}\bar{D}$ BCD

$A\bar{B}\bar{C}$ $A\bar{B}\bar{C}\bar{D}$

$A\bar{B}\bar{C}$ $A\bar{B}$

$A\bar{B}C$ $A\bar{B}$

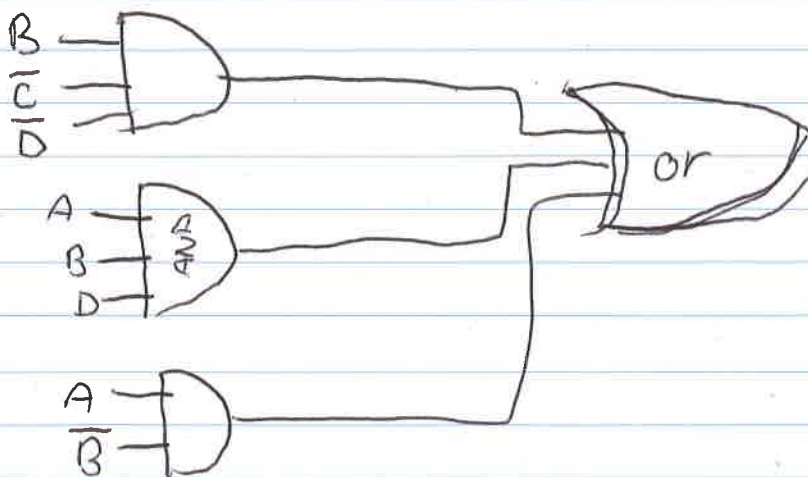
$A\bar{B}C$ $A\bar{B}$

$A\bar{B}\bar{C}$ $A\bar{B}\bar{C}\bar{D}$

$A\bar{B}\bar{C}$ $A\bar{B}D$

$ABCD$ ABD

8 ✓



6 ✓

Q3_ryan.vhd

```

1  -----
2  -- Company:
3  -- Engineer:
4  --
5  -- Create Date:      12:13:53 05/18/2018
6  -- Design Name: Ryan Q3
7  -- Module Name:      Q3_ryan
8  -- Project Name:
9  -- Target Devices:
10 -- Tool versions:
11 -- Description:
12 --
13 -- Dependencies:
14 --
15 -- Revision:
16 -- Revision 0.01 - File Created
17 -- Additional Comments:
18 --
19 -----
20 library IEEE;
21 use IEEE.STD_LOGIC_1164.ALL;
22
23 -- Uncomment the following library declaration if using
24 -- arithmetic functions with Signed or Unsigned values
25 --use IEEE.NUMERIC_STD.ALL;
26
27 -- Uncomment the following library declaration if instantiating
28 -- any Xilinx primitives in this code.
29 --library UNISIM;
30 --use UNISIM.VComponents.all;
31
32 entity Q3_ryan is
33     Port ( Clk : in  STD_LOGIC;
34           W : in  STD_LOGIC;
35           Y : out  STD_LOGIC_VECTOR (2 downto 0));
36 end Q3_ryan;
37
38 architecture Behavioral of Q3_ryan is
39     type state_type (State_1,state_2,state_3,state_4,state_5,state_6,state_7,state_8);
40     signal present_state:state_type;
41     signal next_state:state_type;
42     begin
43     state:process(present_state,W)
44     begin
45         If W='0' then
46             Case pressent_state is
47             when State_1=>next_state<=state_1;Y<='000';
48             when State_2=>next_state<=state_5;Y<='101';
49             when State_3=>next_state<=state_4;Y<='100';
50             when State_4=>next_state<=state_6;Y<='011';
51             when State_5=>next_state<=state_6;Y<='011';
52             when State_6=>next_state<=state_8;Y<='001';
53             when State_7=>next_state<=state_8;Y<='001';
54             when State_8=>next_state<=state_2;Y<='010';
55             others <= null;
56         end case;

```

Q3_ryan.vhd

```
57  else if W='1' then
58  case present_state is
59  when State_1=>next_state<=state_2;Y<='010';
60  when State_2=>next_state<=state_3;Y<='110';
61  when State_3=>next_state<=state_6;Y<='011';
62  when State_4=>next_state<=state_5;Y<='101';
63  when State_5=>next_state<=state_3;Y<='110';
64  when State_6=>next_state<=state_7;Y<='111';
65  when State_7=>next_state<=state_3;Y<='110';
66  when State_8=>next_state<=state_1;Y<='000';
67  end case;
68  end if;
69  end if;
70
71
72  end process state;
73  clock:process(CLK)
74  if (CLK=1) and (clk'last_value=0) then
75  present_state => next_state;
76  end if ;
77  end process clock;
78
79  end Behavioral;
80
81
```

*no others catch all**no begin**(L=)**14*

```
1  -----
2  -- Company:
3  -- Engineer:
4  --
5  -- Create Date:    12:03:55 05/18/2018
6  -- Design Name:    Q4A
7  -- Module Name:    Q4B_RYAN - Behavioral
8  -- Project Name:
9  -- Target Devices:
10 -- Tool versions:
11 -- Description:
12 --
13 -- Dependencies:
14 --
15 -- Revision:
16 -- Revision 0.01 - File Created
17 -- Additional Comments:
18 --
19  -----
20 library IEEE;
21 use IEEE.STD_LOGIC_1164.ALL;
22
23 -- Uncomment the following library declaration if using
24 -- arithmetic functions with Signed or Unsigned values
25 --use IEEE.NUMERIC_STD.ALL;
26
27 -- Uncomment the following library declaration if instantiating
28 -- any Xilinx primitives in this code.
29 --library UNISIM;
30 --use UNISIM.VComponents.all;
31
32 entity Q4A_RYAN is
33     Port ( A : in  STD_LOGIC_VECTOR (2 downto 0);
34           Y : out  STD_LOGIC_VECTOR (6 downto 0));
35 end Q4B_RYAN;
36
37 architecture Behavioral of Q4A_RYAN is
38 begin;
39 DECODE: PROCESS (A)
40 begin;
41 CASE DECODE is
42 WHEN 000 => Y <= 1111110;
43 WHEN 001 => Y <= 1111101;
44 WHEN 010 => Y <= 1111011;
45 WHEN 011 => Y <= 1110111;
46 WHEN 100 => Y <= 1101111;
47 WHEN 110 => Y <= 1011111;
48 WHEN 111 => Y <= 0111111;
49
50 end case
51 end process decode
52
53
54 end Behavioral;
55
56
```

```
1  -----
2  -- Company:
3  -- Engineer:
4  --
5  -- Create Date:    11:28:33 05/18/2018
6  -- Design Name: rYAN o'SULLIVAN
7  -- Module Name:    Q3_ryan - Behavioral
8  -- Project Name: Q4b_ryan
9  -- Target Devices:
10 -- Tool versions:
11 -- Description:
12 --
13 -- Dependencies:
14 --
15 -- Revision:
16 -- Revision 0.01 - File Created
17 -- Additional Comments:
18 --
19  -----
20 library IEEE;
21 use IEEE.STD_LOGIC_1164.ALL;
22
23 -- Uncomment the following library declaration if using
24 -- arithmetic functions with Signed or Unsigned values
25 --use IEEE.NUMERIC_STD.ALL;
26
27 -- Uncomment the following library declaration if instantiating
28 -- any Xilinx primitives in this code.
29 --library UNISIM;
30 --use UNISIM.VComponents.all;
31
32 entity Q3_ryan is
33     Port ( CLK : in  STD_LOGIC;
34           W  : in  STD_LOGIC;
35           Y  : out STD_LOGIC);
36 end Q3_ryan;
37
38 architecture Behavioral of Q4b_ryan is
39     type state_type (State_A,state_B,state_C,state_D,state_E,state_F,state_G);
40     signal present_state:state_type;
41     signal next_state:state_type;
42     begin
43     state:process(present_state,W)
44     begin
45     If W='0' then
46     Case pressent_state is
47     when State_A=>next_state<=state_A;Y<='0';
48     when State_B=>next_state<=state_C;Y<='0';
49     when State_C=>next_state<=state_C;Y<='0';
50     when State_D=>next_state<=state_E;Y<='0';
51     when State_E=>next_state<=state_A;Y<='0';
52     when State_F=>next_state<=state_G;Y<='0';
53     when State_G=>next_state<=state_A;Y<='1';
54     others <= null;
55     end case;
56
```

Q4B

Fri May 18 12:00:00 2018

99_ryan.vhd

```

57  else if W='1' then
58  case present_state is
59  when State_A=>next_state<=state_B;Y<='0';
60  when State_B=>next_state<=state_C;Y<='0';
61  when State_C=>next_state<=state_D;Y<='1';
62  when State_D=>next_state<=state_F;Y<='1';
63  when State_E=>next_state<=state_A;Y<='0';
64  when State_F=>next_state<=state_F;Y<='0';
65  when State_G=>next_state<=state_A;Y<='1';
66  end case;
67  end if;
68  end if;
69
70  end process state;
71  clock:process(CLK)
72  if (CLK=1) and (clk'last_value=0) then
73  present_state => next_state;
74  end if ;
75  end process clock;
76
77  end Behavioral;
78
79

```

no begin
Assignment <=
⑤ /
① /